ABSTRACT
IEEE 754r is the ongoing revision to the IEEE 754 floating point standard and a major enhancement to the standard is the addition of decimal format. Firstly, this paper proposes novel two transistor AND & OR gates. The proposed AND gate has no power supply, thus it can be referred as the Powerless AND gate. Similarly, the proposed two transistor OR gate has no ground and can be referred as Groundless OR. Two designs of AND & OR gate without VDD or GND are also shown. Secondly for IEEE 754r format, one novel BCD adder called carry look-ahead BCD adder is also proposed. In order to design the carry look-ahead BCD adder, a novel 4 bit carry look-ahead adder called NCLA is proposed which forms the basic building block of the proposed carry look-ahead BCD adder. The proposed two transistors AND & OR gates are used to provide the optimized small area, low power, high throughput circuitries of the proposed BCD adder. Nowadays, reversible logic is also emerging as a promising computing paradigm having its implementation of the proposed BCD adder in terms of small transistors AND & OR gates are used to provide the optimized small area, low power and high throughput circuitry.

IN INTRODUCTION
Nowadays, the decimal arithmetic is receiving significant attention as the financial, commercial, and Internet-based applications cannot tolerate errors generated by conversion between decimal and binary formats. Furthermore, a number of decimal numbers, such as 0.110, cannot be exactly represented. Reversible Logic. Thus, reversible logic implementation of the proposed BCD adder is also shown in this paper. Keywords
BCD Arithmetic, BCD Adders, Two Transistors AND/OR Gate, Reversible Logic.

1. INTRODUCTION
Nowadays, the decimal arithmetic is receiving significant attention as the financial, commercial, and Internet-based applications cannot tolerate errors generated by conversion between decimal and binary formats. Furthermore, a number of decimal numbers, such as 0.110, cannot be exactly represented. Reversible Logic. Thus, reversible logic implementation of the proposed BCD adder is also shown in this paper. Keywords
BCD Arithmetic, BCD Adders, Two Transistors AND/OR Gate, Reversible Logic.

1. INTRODUCTION
Nowadays, the decimal arithmetic is receiving significant attention as the financial, commercial, and Internet-based applications cannot tolerate errors generated by conversion between decimal and binary formats. Furthermore, a number of decimal numbers, such as 0.110, cannot be exactly represented. Reversible Logic. Thus, reversible logic implementation of the proposed BCD adder is also shown in this paper. Keywords
BCD Arithmetic, BCD Adders, Two Transistors AND/OR Gate, Reversible Logic.

1. INTRODUCTION
Nowadays, the decimal arithmetic is receiving significant attention as the financial, commercial, and Internet-based applications cannot tolerate errors generated by conversion between decimal and binary formats. Furthermore, a number of decimal numbers, such as 0.110, cannot be exactly represented. Reversible Logic. Thus, reversible logic implementation of the proposed BCD adder is also shown in this paper. Keywords
BCD Arithmetic, BCD Adders, Two Transistors AND/OR Gate, Reversible Logic.

1. INTRODUCTION
Nowadays, the decimal arithmetic is receiving significant attention as the financial, commercial, and Internet-based applications cannot tolerate errors generated by conversion between decimal and binary formats. Furthermore, a number of decimal numbers, such as 0.110, cannot be exactly represented. Reversible Logic. Thus, reversible logic implementation of the proposed BCD adder is also shown in this paper. Keywords
BCD Arithmetic, BCD Adders, Two Transistors AND/OR Gate, Reversible Logic.
and quantum computing. Quantum arithmetic must be built from reversible logical components.

One of the major constraints in reversible logic is to minimize the reversible gate used and garbage output produced (gate output that are added to maintain the reversibility but are not used in further computations). This paper also introduces the reversible implementation of the proposed CLA BCD adder using existing reversible gates such as TSG[15], Fredkin(F)[12,13,14], Feynman(FG)[12,13] and R2 gate[17].

The design strategy is chosen in such a way that the proposed reversible implementation of the CLA BCD adder is with minimal number of reversible gates and garbage outputs. Thus, an attempt has also been tried to design optimal reversible BCD adder to provide the platform for building decimal ALU of a Quantum CPU.

2. TWO TRANSISTOR AND/OR GATES

In this paper, novel two transistor AND & OR gates are proposed. The proposed two transistors AND gate is shown in Figure 1. It has no power supply, thus it can be referred as the Powerless AND gate. Similarly, two transistor OR gate is proposed as shown in Figure 2, having no ground and can be referred as Groundless OR gate. As far as the survey of literature and our knowledge is concerned, these are the most optimal designs of the AND & OR gates which are directly scalable to higher inputs by cascading. Another possible designs of the AND & OR gates without any VDD and GND are shown in Figure 3 & Figure 4.

![Figure 1. Proposed Two Transistor AND Gate](image1)

![Figure 2. Proposed Two Transistor OR Gate](image2)

![Figure 3. Proposed Two Transistor AND Gate Without VDD & GND](image3)

![Figure 4. Proposed Two Transistor AND Gate Without VDD & GND](image4)

Figure 4. Proposed Two Transistor AND Gate Without VDD & GND

The evaluation of the proposed architectures is done both theoretically as well as experimentally through SPICE simulations. The following equation [5,19] is used to estimate the power consumption of a circuit.

\[
P_{\text{dynamic}} = (\sum_i C_i V_{\text{swing}} P_i f_{\text{clk}} + I_{\text{leak}} V_{\text{DD}} + \sum_i I_{\text{leak}} V_{\text{DD}})
\]

In the above equation, \(P_{\text{dynamic}}\) is the power consumption, \(C_i\) is the load capacitance, \(V_i\) is the voltage swing, \(P_i\) is the probability of a switch, \(f_{\text{clk}}\) is the clock frequency, \(I_{\text{leak}}\) is the short-circuit current, \(I_{\text{leak}}\) is the leakage current and \(V_{\text{DD}}\) is the supply voltage. It can be inferred from the above equation that the main components of the power dissipation are the \(I_{\text{leak}}\) and \(V_{\text{swing}}\) components. Since, the \(I_{\text{leak}}\) component in the equation is usually very low and is generally discarded. The voltage swing of a circuit is referred as the change in voltage during a transition and is equal to the voltage difference between logic ‘1’ and logic ‘0’ [19]. The reduction in voltage swing results in lower power dissipation [19] and there is a reduction in the voltage swing when the signals are not fully transmitted (when NMOS transmits logic ‘1’ and a PMOS transmits logic ‘0’) [6,8,19].

The proposed AND & OR gate have incomplete voltage swings since in the proposed AND gate (Fig.1) PMOS is permanently tied to logic ‘0’ and in the proposed OR gate (Fig. 2) NMOS is permanently tied to logic ‘1’. Moreover, since the proposed gates have only either VDD or GND, neither both in the same circuit, there is no short-circuit current established by a direct path between VDD and GND. Thus the proposed gates are highly optimized in terms of power consumption.

3. EXPERIMENT DESCRIPTION

The simulation environment is setup to measure the performance of the proposed circuits in terms of propagation delay and power dissipation. The simulations are performed by varying the frequencies and the capacitive loads to ensure that the proposed circuits work at different frequencies and different capacitive loads. The Simulation conditions are shown in Figure 5.

![Figure 5. Simulation Conditions](image5)

The simulation is done in Tanner spice and the technology being used is 0.35-um CMOS digital technology (TSMC 35, Canadian Microelectronic Corporation) with a 3.3-V supply voltage. The propagation delay is measured when the changing input reaches 50% of the transition to the time when the output reaches its 50%. Figure 6 and Figure 7 shows the propagation delay and the power consumption for a load of 0.01pf at different frequencies. Similarly results have been obtained for the other loading conditions. Since the proposed gates are implemented with the bare minimum of two transistors and are most optimal, hence no comparative study is shown.
4. PROPOSED NEW CARRY LOOK-AHEAD (NCLA) ADDER

Recently, a modified carry look-ahead adder [7] (abbreviated as MCLA) is proposed which is similar to CLA (carry look-ahead adder) in basic construction. The MCLA circuit in [7] uses NAND gates to replace the AND, OR, and NOT gates in the conventional CLA to decrease the cost and increase the speed. It can be easily inferred from the design of MCLA [7] that in spite of having significant speed improvement, it has significant increase in area due to excessive number of NAND gates used for the faster carry propagation. This problem will significantly increase when the MCLA will be cascaded for designing higher order CLA. Thus, the authors propose a new CLA architecture called NCLA emphasizing the use of proposed AND & OR gates instead of NAND gates. It has already been proved above that the proposed AND & OR gates are highly optimized in terms of area, low power and speed. Thus, implementing the AND & OR functions in the conventional CLA with the proposed AND and OR gates will significantly increase its performance compared to MCLA using NAND gates, in terms of area, power and throughput. The proposed NCLA will consist of PGA (propagate generate architecture) block that is used to generate Si, Gi and Pi as shown in Figure 8. The proposed 4-bit NCLA adder is shown in Figure 9, in which at the 4th place full adder is used instead of PGA. This is done to reduce the area (number of gates) of the NCLA without sacrificing the speed improvement found in MCLA. It can be easily verified that there will be reduction of number of gates to generate the final carry as shown in Figure 9. Using the proposed AND & OR gates, the number of transistors required to implement the proposed NCLA are 74 compared to the use of 136 transistors in MCLA proposed in [7]. The Comparison is clearly explained below and the Table I show the number of transistors required to implement the various logic operations.

<table>
<thead>
<tr>
<th>Logic Function</th>
<th>Number of Transistors Required</th>
</tr>
</thead>
<tbody>
<tr>
<td>NOT Gate</td>
<td>2</td>
</tr>
<tr>
<td>2 input XOR gate</td>
<td>4</td>
</tr>
<tr>
<td>2 input NAND gate</td>
<td>4</td>
</tr>
<tr>
<td>3 input NAND gate</td>
<td>6</td>
</tr>
<tr>
<td>4 input NAND gate</td>
<td>8</td>
</tr>
<tr>
<td>1 bit full adder[8]</td>
<td>10</td>
</tr>
<tr>
<td>1 bit multiplexer based full adder without any Power supply[4]</td>
<td>12</td>
</tr>
<tr>
<td>Proposed 2 input AND gate</td>
<td>2</td>
</tr>
<tr>
<td>Proposed 2 input OR gate</td>
<td>2</td>
</tr>
<tr>
<td>3 input AND gate designed by cascading proposed AND gate</td>
<td>4</td>
</tr>
<tr>
<td>4 input AND gate designed by cascading the proposed AND gate</td>
<td>6</td>
</tr>
<tr>
<td>4 input OR gate designed by cascading the proposed AND gate</td>
<td>6</td>
</tr>
</tbody>
</table>

The metamorphosis of partial full adder (MPFA) in [7] generating (Si, Gi, Pi) requires two two-input XOR gate and one two-input NAND gate leading to the total number of 12 transistors as shown below

\[
2 \times 2_{\text{Ex-Or}} + 1 \times 2_{\text{NAND}} = 12 \text{ transistors}
\]

Table II shows that the total number of transistors required to implement the fastest CLA called MCLA is 136.

<table>
<thead>
<tr>
<th>Blocks</th>
<th>Number of Transistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>4 MPFA</td>
<td>12 \times 4 = 48</td>
</tr>
<tr>
<td>3 NOT</td>
<td>3 \times 2 = 6</td>
</tr>
<tr>
<td>5 two input NAND</td>
<td>5 \times 4 = 20</td>
</tr>
<tr>
<td>4 three input NAND</td>
<td>4 \times 6 = 24</td>
</tr>
<tr>
<td>4 four input NAND</td>
<td>4 \times 8 = 32</td>
</tr>
<tr>
<td>1 four input AND</td>
<td>6</td>
</tr>
<tr>
<td><strong>Total Number of Transistor</strong></td>
<td><strong>136</strong></td>
</tr>
</tbody>
</table>

The proposed NCLA in this paper requires 74 transistors as shown in the Table III.

<table>
<thead>
<tr>
<th>Gates</th>
<th>Number of Transistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>3 1 bit NFA</td>
<td>3 \times 10 = 30</td>
</tr>
<tr>
<td>3 two input AND gate</td>
<td>3 \times 2 = 6</td>
</tr>
<tr>
<td>2 three input AND gate</td>
<td>2 \times 4 = 8</td>
</tr>
<tr>
<td>1 four input AND gate</td>
<td>6</td>
</tr>
<tr>
<td>Inputs</td>
<td>Transistor Count</td>
</tr>
<tr>
<td>--------</td>
<td>------------------</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>4</td>
<td>6</td>
</tr>
<tr>
<td>1 bit</td>
<td>12</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>74</strong></td>
</tr>
</tbody>
</table>

Thus, it can be easily inferred from Table II and Table III that the proposed NCLA is highly beneficial in number of transistors, thus in terms of area, speed and power compared to MCLA proposed in [7]. Figure 13 shows the transistor implementation of the PGA in which XOR gate proposed in [9,19] is used and Figure 14 shows the transistor implementation of the proposed NCLA in which the fourth block full adder is the multiplexer based low power adder proposed in [4]. The multiplexer based adder is used to further improve the speed and have the more power saving in NCLA. The proposed 4-bit NCLA is used to design optimized CLA BCD adder as explained in the next section. The functional verification of the NCLA is done using Verilog HDL at gate level and using SPICE at transistor level.

5. PROPOSED CARRY LOOK-AHEAD BCD ADDER

In this paper, the authors also propose a novel Carry Look-Ahead BCD Adder which is suitable for CMOS implementation as well as reversible logic implementation. In the proposed CLA BCD adder, the 4-bit adders used in the conventional BCD adder are replaced by the proposed 4-bit NCLA. The two decimal digits, together with the input carry, are first added in the top 4-bit NCLA to produce the binary sum. When the output carry is equal to zero, nothing is added to the binary sum. When it is equal to one, binary 0110 is added to the binary sum using another 4-bit NCLA (bottom NCLA). The output carry generated from the bottom NCLA is ignored, since it supplies information already available at the output carry terminal. Furthermore, the OR & AND function used in the conventional BCD adder are implemented with the proposed two transistors AND & OR gates. Figure 15(a) shows the proposed CLA BCD adder and Figure 15(b) show the transistor implementation of the proposed CLA BCD adder using proposed AND and OR gates. The functional verification of the proposed CLA BCD adder is done in Verilog HDL at gate level using Model Sim and at transistor level using TSPICE at 0.35 micron TSMC library.

6. REVERSIBLE DESIGN OF THE PROPOSED CARRY LOOK-AHEAD BCD ADDER

As evident from the Figure 15, in order to have the reversible design of the proposed carry look-ahead BCD Adder; reversible design of the NCLA is required. In carry look-ahead adder, we consider two new binary variables:

\[
P_i = A_i \oplus B_i \\
G_i = A_i B_i
\]

Then, the output sum and carry of full adder can be rewritten as follows:

\[
S_i = A_i \oplus B_i \oplus C_i \\
C_{i+1} = A_i B_i + (A_i \oplus B_i) C_i = A_i B_i (A_i \oplus B_i) C_i = G_i P_i C_i
\]

The 4-bit reversible Carry look-ahead adder is created by expanding the above equations.

\[
C_1 = G_0 \oplus P_0 C_0 \\
C_2 = G_1 \oplus P_1 C_1 + G_1 + P_1 G_0 + P_1 P_0 C_0 \\
C_3 = G_2 \oplus P_2 C_2 + G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0
\]

In the proposed 4-bit reversible carry look-ahead adder, the Pi, Gi and Si are generated from reversible TSG gate[15] and Fredkin gate[12,13,14]. The block generating Pi, Gi and Si is called PGA (Carry Propagate & Carry Generate Adder). The structure of PGA is shown in Fig. 10 and the complete structure of the 4-bit carry look-ahead adder is shown in Fig. 11. In the complete design of CLA in Fig. 11 appropriate gates are used wherever required for generating the function with minimum number of reversible gates and garbage outputs. The unused output in Fig. 11 represents the garbage outputs. After designing the reversible NCLA as shown in Fig.11, it is used along with New gate(NG) [18] to design the proposed reversible carry look-ahead BCD Adder as shown in Fig. 12. The choice of the optimal gates at the appropriate places has made the design highly optimal in terms of number of reversible gates and garbage outputs.
7. CONCLUSIONS

The focus of this paper is the IEEE 754r which is the ongoing revision to the IEEE 754 floating point standard considering decimal arithmetic. Thus, this paper proposes two transistors AND & OR gates for small area low power high throughput circuitries. Novel design of BCD adder called Carry Look Ahead BCD Adder is proposed in this paper to cater the need of IEEE 754r format. A novel 4-bit carry look-ahead adder called NCLA is proposed which is used to design the carry look-ahead BCD adder. The optimize transistor implementation of the proposed BCD adder is presented using the proposed AND & OR gates. Finally, the optimal reversible design of the proposed BCD adder is also demonstrated.

REFERENCES

Figure 13. Transistor implementation of PGA

Figure 14. Transistor Implementation of NCLA using proposed AND and OR gates and Multiplexer based full adder

Figure 15. (a) Proposed CLA BCD Adder (b) Transistor implementation of the proposed CLA BCD adder