

Modified Carry Look Ahead BCD Adder With CMOS and Reversible Logic Implementation

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ABSTRACT

IEEE 754r is the ongoing revision to the IEEE 754 floating point standard and a major enhancement to the standard is the addition of decimal format. Firstly, this paper proposes novel two transistor AND & OR gates. The proposed AND gate has no power supply, thus it can be referred as the Powerless AND gate. Similarly, the proposed two transistor OR gate has no ground and can be referred as Groundless OR. Two designs of AND & OR gate without VDD or GND are also shown. Secondly for IEEE 754r format, one novel BCD adder called carry look-ahead BCD adder is also proposed. In order to design the carry look-ahead BCD adder, a novel 4 bit carry look-ahead adder called NCLA is proposed which forms the basic building block of the proposed carry look-ahead BCD adder. The proposed two transistors AND & OR gates are used to provide the optimized small area, low power, high throughput circuitries of the proposed BCD adder. Nowadays, reversible logic is also emerging as a promising computing paradigm having its applications in quantum computing, optical computing and nanotechnology. Thus, reversible logic implementation of the proposed BCD Adder is also shown in this paper.

Keywords

BCD Arithmetic, BCD Adders, Two Transistors AND/OR Gate, Reversible Logic.

1. INTRODUCTION

Nowadays, the decimal arithmetic is receiving significant attention as the financial, commercial, and Internet-based applications cannot tolerate errors generated by conversion between decimal and binary formats. Furthermore, a number of decimal numbers, such as 0.110, cannot be exactly represented in binary, thus, these applications often store data in decimal format and process data using decimal arithmetic software [1]. The advantage of decimal arithmetic in eliminating conversion errors also comes with a drawback; it is typically 100 to 1,000 times slower than binary arithmetic implemented in hardware.

Since, the decimal arithmetic is getting significant attention; specifications for it have recently been added to the draft revision of the IEEE 754 standard for Floating-Point Arithmetic. IEEE 754r is an ongoing revision to the IEEE 754 floating point standard [2,3]. Some of the major enhancements so far incorporated are the addition of 128-bit and decimal formats. Furthermore, three new decimal formats are described, matching the lengths of the binary formats. These have led to the decimal formats with 7, 16, and 34-digit significands, which may be normalized or unnormalized. In the proposed IEEE 754r format, for maximum range and precision, the formats merge part of the exponent and significand into a combination field, and compress the remainder of the significand using densely packed decimal encoding [2,3]. It is anticipated that once the IEEE 754r Standard is finally approved, hardware support for decimal floating-point arithmetic on the processors will come into

existence for financial, commercial, and Internet-based applications. Still, the major consideration while implementing BCD arithmetic will be to enhance its speed as much as possible.

Now from the silicon point of view, in order to satisfy the Moore's law and the high speed processing needs, more and more logic elements are packed into smaller volumes and are clocked at higher frequencies leading to heavy power dissipation as heat. This huge dissipation of power as heat leads to exhaustion of batteries of portable systems and systems overheat [4]. Thus, today there is an increasing need of the portable applications requiring small-area, low-power and high throughput circuitry.

In order to satisfy all the aforesaid expectations; firstly, this paper introduces novel two transistors AND & OR gates. The proposed two transistor AND & OR gates have only either VDD or GND, thus preventing the flow of short circuit current. Another design of the AND & OR gate without any VDD and GND is also shown. Secondly, novel BCD adder architecture termed CLA BCD adder (Carry Look-Ahead) is also proposed. In order to propose the novel CLA BCD adder, a new 4-bit carry look-ahead architecture called NCLA is proposed which is better than the fastest CLA [7], in terms of area while maintaining the speed improvement of the fastest CLA. The proposed two transistors AND & OR gates are used to provide the optimize implementation of the proposed BCD adder in terms of small area, low power and high throughput.

Moreover, researchers like Landauer have shown that for irreversible logic computations, each bit of information lost, generates $kT \ln 2$ joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which computation is performed [10]. Bennett showed that $kT \ln 2$ energy dissipation would not occur, if a computation is carried out in a reversible way [11], since the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. Reversible circuits are those circuits that do not lose information and reversible computation in a system can be performed only when the system comprises of reversible gates. These circuits can generate unique output vector from each input vector, and vice versa, that is, there is a one-to-one mapping between input and output vectors. Thus, an $N \times N$ reversible gate can be represented as

$$I_v = (I_1, I_2, I_3, I_4, \dots, I_N)$$

$$O_v = (O_1, O_2, O_3, \dots, O_N)$$

Where I_v and O_v represent the input and output vectors respectively. Classical logic gates are irreversible since input vector states cannot be uniquely reconstructed from the output vector states. There are a number of existing reversible gates such as Fredkin gate [12,13,14], Toffoli Gate (TG) [12,13] and the New Gate (NG) [18]. The reversible logic operations do not erase (lose) information and dissipate very less heat. Thus, reversible logic is likely to be in demand in high speed power aware circuits. Reversible circuits are also of high interest in low-power CMOS design, optical computing, nanotechnology

and quantum computing. Quantum arithmetic must be built from reversible logical components.

One of the major constraints in reversible logic is to minimize the reversible gate used and garbage output produced (gate output that are added to maintain the reversibility but are not used in further computations). This paper also introduces the reversible implementation of the proposed CLA BCD adder using existing reversible gates such as TSG[15], Fredkin(F)[12,13,14], Feynman(FG)[12,13] and R2 gate[17].

The design strategy is chosen in such a way that that the proposed reversible implementation of the CLA BCD adder is with minimal number of reversible gates and garbage outputs. Thus, an attempt has also been tried to design optimal reversible BCD adder to provide the platform for building decimal ALU of a Quantum CPU.

2. TWO TRANSISTOR AND/OR GATES

In this paper, novel two transistor AND & OR gates are proposed. The proposed two transistor AND gate is shown in Figure 1. It has no power supply, thus it can be referred as the Powerless AND gate. Similarly, two transistor OR gate is proposed as shown in Figure 2, having no ground and can be referred as Groundless OR gate. As far as the survey of literature and our knowledge is concerned, these are the most optimal designs of the AND & OR gates which are directly scalable to higher inputs by cascading. Another possible designs of the AND & OR gates without any VDD and GND are shown in Figure 3 & Figure 4.

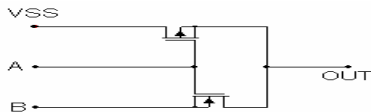


Figure 1. Proposed Two Transistor AND Gate

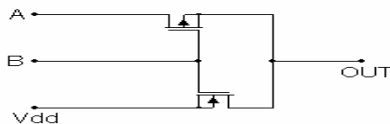


Figure 2. Proposed Two Transistor OR Gate

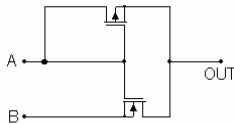


Figure 3. Proposed Two Transistor AND Gate Without VDD & GND

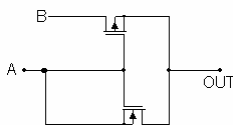


Figure 4. Proposed Two Transistor AND Gate Without VDD & GND

The evaluation of the proposed architectures is done both theoretically as well as experimentally through SPICE simulations. The following equation [5,19] is used to estimate the power consumption of a circuit.

$$P_{Dynamic} = (\sum_i C_i * V_{i_swing} * P_i) * f_{clk} + I_{sc} * VDD + \sum_i I_{leak} * VDD$$

In the above equation, $P_{Dynamic}$ is the power consumption, C_i is the load capacitance, V_i is the voltage swing, P_i is the probability of a switch, f_{clk} is the clock frequency, I_{sc} is the short-circuit current, I_{leak} is the leakage current and VDD is the supply voltage. It can be inferred from the above equation that the main components of the power dissipation are the I_{sc} and V_{swing} components. Since, the I_{leak} component in the equation is usually very low and is generally discarded. The voltage swing of a circuit is referred as the change in voltage during a transition and is equal to the voltage difference between logic '1' and logic '0' [19]. The reduction in voltage swing results in lower power dissipation [19] and there is a reduction in the voltage swing when the signals are not fully transmitted (when NMOS transmits logic '1' or a PMOS transmits logic '0')[6,8,19].

The proposed AND & OR gate have incomplete voltage swings since in the proposed AND gate (Fig.1) PMOS is permanently tied to logic '0' and in the proposed OR gate (Fig. 2) NMOS is permanently tied to logic '1'. Moreover, since the proposed gates have only either VDD or GND, neither both in the same circuit, there is no short-circuit current established by a direct path between VDD and VSS. Thus the proposed gates are highly optimized in terms of power consumption.

3. EXPERIMENT DESCRIPTION

The simulation environment is setup to measure the performance of the proposed circuits in terms of propagation delay and power dissipation. The simulations are performed by varying the frequencies and the capacitive loads to ensure that the proposed circuits work at different frequencies and different capacitive loads. The Simulation conditions are shown in Figure 5.

Load	0.01 pf	0.02 pf	0.05 pf	0.1 pf	0.3 pf	0.5 pf
Frequencies	1 Mhz	50 Mhz	100 Mhz	200 Mhz		

Figure 5. Simulation Conditions

The simulation is done in Tanner spice and the technology being used is 0.35-um CMOS digital technology (TSMC 35, Canadian Microelectronic Corporation) with a 3.3-V supply voltage. The propagation delay is measured when the changing input reaches 50% of the transition to the time when the output reaches its 50%. Figure 6 and Figure 7 shows the propagation delay and the power consumption for a load of 0.01pf at different frequencies. Similarly results have been obtained for the other loading conditions. Since the proposed gates are implemented with the bare minimum of two transistors and are most optimal, hence no comparative study is shown.

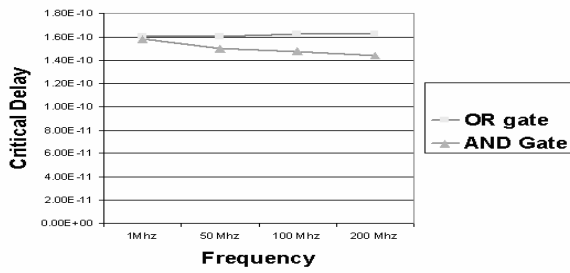


Figure 6. Critical Delay of Proposed Circuits(Seconds) at 0.01pf

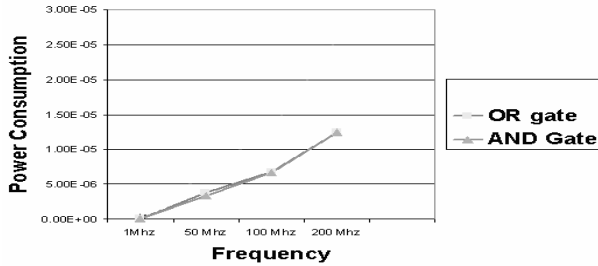


Figure 7. Power Consumption of Proposed Circuits(Watts) at 0.01pf

4. PROPOSED NEW CARRY LOOK-AHEAD (NCLA) ADDER

Recently, a modified carry look-ahead adder [7] (abbreviated as MCLA) is proposed which is similar to CLA (carry look-ahead adder) in basic construction. The MCLA circuit in [7] uses NAND gates to replace the AND, OR and NOT gates in the conventional CLA to decrease the cost and increase the speed. It can be easily inferred from the design of MCLA [7] that in spite of having significant speed improvement, it has significant increase in area due to excessive number of NAND gates used for the faster carry propagation. This problem will significantly increase when the MCLA will be cascaded for designing higher order CLA. Thus, the authors propose a new CLA architecture called NCLA emphasizing the use of proposed AND & OR gates instead of NAND gates. It has already been proved above that the proposed AND & OR gates are highly optimized in terms of area, low power and speed. Thus, implementing the AND & OR functions in the conventional CLA with the proposed AND and OR gates will significantly increase its performance compared to MCLA using NAND gates, in terms of area, power and throughput. The proposed NCLA will consist of PGA(propagate generate architecture) block that is used to generate Si, Gi and Pi as shown in Figure 8. The proposed 4-bit NCLA adder is shown in Figure 9, in which at the 4th place full adder is used instead of PGA. This is done to reduce the area (number of gates) of the NCLA without sacrificing the speed improvement found in MCLA. It can be easily be verified that there will be reduction of number of gates to generate the final carry as shown in the Figure 9. Using the proposed AND & OR gates, the number of transistors required to implement the proposed NCLA are 74 compared to the use of 136 transistors in MCLA proposed in [7]. The Comparison is clearly explained below and the Table I show the number of transistors required to implement the various logic operations.

TABLE I. NUMBER OF TRANSISTORS REQUIRED TO PERFORM THE LOGIC OPERATIONS

Logic Function	Number of Transistors Required
NOT Gate	2
2 input XOR gate	4
2 input NAND gate	4
3 input NAND gate	6
4 input NAND gate	8
1 bit full adder[8]	10
1 bit multiplexer based full adder without any Power supply[4]	12
Proposed 2 input AND gate	2
Proposed 2 input OR gate	2
3 input AND gate designed by cascading proposed AND gate	4
4 input AND gate designed by cascading the proposed AND gate	6
4 input OR gate designed by cascading the proposed AND gate	6

The metamorphosis of partial full adder(MPFA) in [7] generating (Si,Gi,Pi) requires two two-input XOR gate and one two-input NAND gate leading to the total number of 12 transistors as shown below

$$2 \text{ 2_Ex-Or}$$

$$1 \text{ 2_NAND}$$

$$\Rightarrow 2*(4) + 1*(4) = 12 \text{ transistors.}$$

Table II shows that the total number of transistors required to implement the fastest CLA called MCLA is 136.

TABLE II. NUMBER OF TRANSISTORS REQUIRED TO IMPLEMENT MCLA[7]

Blocks	Number of Transistors
4 MPFA	12 * 4= 48
3 NOT	3 *2=6
5 two input NAND	5*4=20
4 three input NAND	4*6=24
4 four input NAND	4 *8=32
1 four input AND	6
Total Number of Transistor	136

The proposed NCLA in this paper requires 74 transistors as shown in the Table III.

TABLE III. NUMBER OF TRANSISTORS REQUIRED TO IMPLEMENT NCLA

Gates	Number of Transistors
3 1 bit NFA	3 * 10=30
3 two input AND gate	3 *2=6
2 three input AND gate	2 *4=8
1 four input AND gate	6

1 two input OR gate	2
1 three input OR gate	4
1 four input OR gate	6
1 bit Adder	12
Total number of Transistors	74

Thus, it can be easily inferred from Table II and Table III that the proposed NCLA is highly beneficial in number of transistors, thus in terms of area, speed and power compared to MCLA proposed in [7]. Figure 13 shows the transistor implementation of the PGA in which XOR gate proposed in [9,19] is used and Figure 14 shows the transistor implementation of the proposed NCLA in which the fourth block full adder is the multiplexer based low power adder proposed in [4]. The multiplexer based adder is used to further improve the speed and have the more power saving in NCLA. The proposed 4-bit NCLA is used to design optimized CLA BCD adder as explained in the next section. The functional verification of the NCLA is done using Verilog HDL at gate level and using SPICE at transistor level.

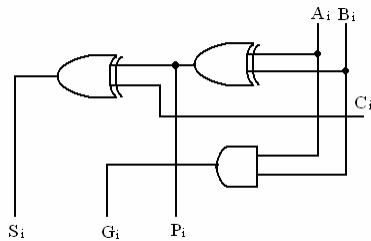


Figure 8. PGA Block generating S_i , G_i and P_i

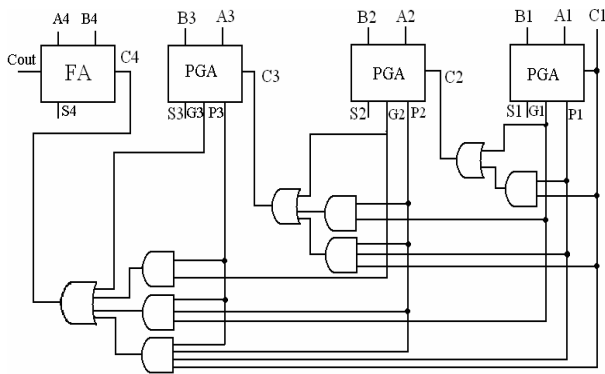


Figure 9. Proposed 4-bit NCLA

5. PROPOSED CARRY LOOK-AHEAD BCD ADDER

In this paper, the authors also propose a novel Carry Look-Ahead BCD Adder which is suitable for CMOS implementation as well as reversible logic implementation. In the proposed CLA BCD adder, the 4-bit adders used in the conventional BCD adder are replaced by the proposed 4-bit NCLA. The two decimal

digits, together with the input carry, are first added in the top 4-bit NCLA to produce the binary sum. When the output carry is equal to zero, nothing is added to the binary sum. When it is equal to one, binary 0110 is added to the binary sum using another 4-bit NCLA (bottom NCLA). The output carry generated from the bottom NCLA is ignored, since it supplies information already available at the output carry terminal. Furthermore, the OR & AND function used in the conventional BCD adder are implemented with the proposed two transistors AND & OR gates. Figure 15(a) shows the proposed CLA BCD adder and Figure 15(b) show the transistor implementation of the proposed CLA BCD adder using proposed AND and OR gates. The functional verification of the proposed CLA BCD adder is done in Verilog HDL at gate level using Model Sim and at transistor level using TSPICE at 0.35 micron TSMC library.

6. REVERSIBLE DESIGN OF THE PROPOSED CARRY LOOK-AHEAD BCD ADDER

As evident from the Figure 15, in order to have the reversible design of the proposed carry look-ahead BCD Adder; reversible design of the NCLA is required. In carry look-ahead adder, we consider two new binary variables:

$$P_i = A_i \oplus B_i$$

$$G_i = A_i B_i$$

Then, the output sum and carry of full adder can be rewritten as follows:

$$S_i = A_i \oplus B_i \oplus C_i = P_i \oplus C_i$$

$$C_{i+1} = A_i B_i + (A_i \oplus B_i) C_i = A_i B_i \oplus (A_i \oplus B_i) C_i = G_i \oplus P_i C_i$$

The 4 bit reversible Carry look-ahead adder is created by expanding the above equations.

$$C_1 = G_0 \oplus P_0 C_0$$

$$C_2 = G_1 \oplus P_1 C_1 = G_1 \oplus P_1 G_0 \oplus P_1 P_0 C_0$$

$$C_3 = G_2 \oplus P_2 C_2 = G_2 \oplus P_2 G_1 \oplus P_2 P_1 G_0 \oplus P_2 P_1 P_0 C_0$$

In the proposed 4-bit reversible carry look-ahead adder, the P_i , G_i and S_i are generated from reversible TSG gate[15] and Fredkin gate[12,13,14]. The block generating P_i , G_i and S_i is called PGA (Carry Propagate & Carry Generate Adder). The structure of PGA is shown in Fig. 10 and the complete structure of the 4-bit carry look-ahead adder is shown in Fig. 11. In the complete design of CLA in Fig. 11 appropriate gates are used wherever required for generating the function with minimum number of reversible gates and garbage outputs. The unused output in Fig. 11 represents the garbage outputs. After designing the reversible NCLA as shown in Fig.11, it is used along with New gate(NG) [18] to design the proposed reversible carry look-ahead BCD Adder as shown in Fig. 12. The choice of the optimal gates at the appropriate places has made the design highly optimal in terms of number of reversible gates and garbage outputs.

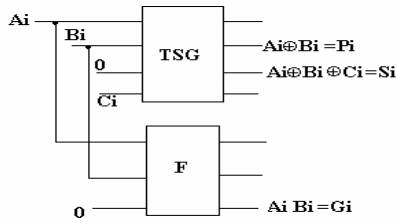


Figure 10. PGA Block in CLA generating Sum, Pi and Gi Using TSG and Fredkin Gate(F)

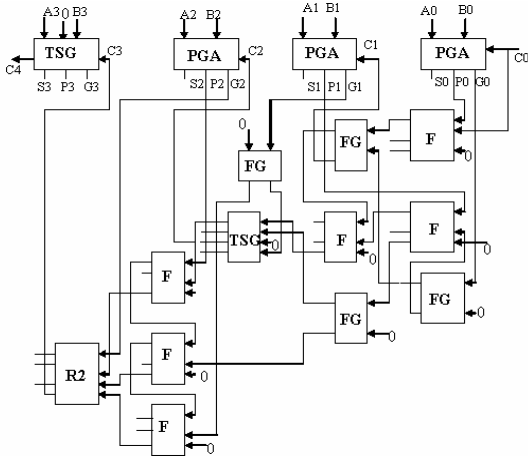


Figure 11. Reversible CLA Designed with TSG, Fredkin(F), Feynman(FG) and R2 gate

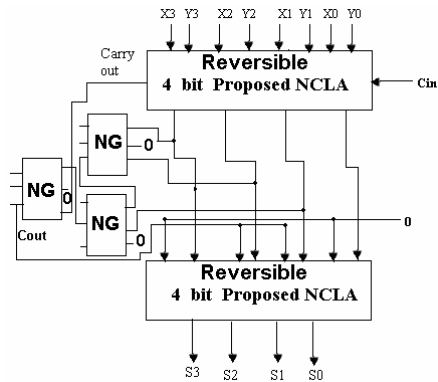


Figure 12. Proposed Reversible BCD Adder

7. CONCLUSIONS

The focus of this paper is the IEEE 754r which is the ongoing revision to the IEEE 754 floating point standard considering decimal arithmetic. Thus, this paper proposes two transistors AND & OR gates for small area low power high throughput circuitries. Novel design of BCD adder called Carry Look Ahead BCD Adder is proposed in this paper to cater the need of IEEE 754r format. A novel 4-bit carry look-ahead adder called NCLA is proposed which is used to design the carry look-ahead BCD adder. The optimize transistor implementation of the proposed BCD adder is presented using the proposed AND & OR gates. Finally, the optimal reversible design of the proposed BCD adder is also demonstrated.

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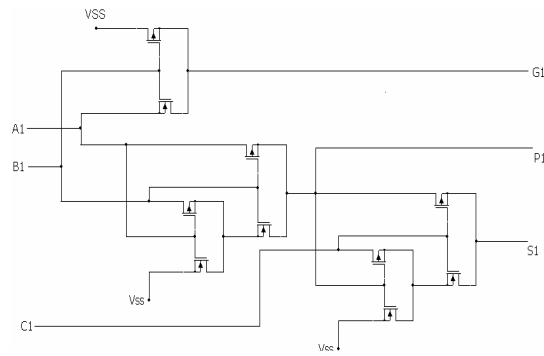


Figure 13. Transistor implementation of PGA

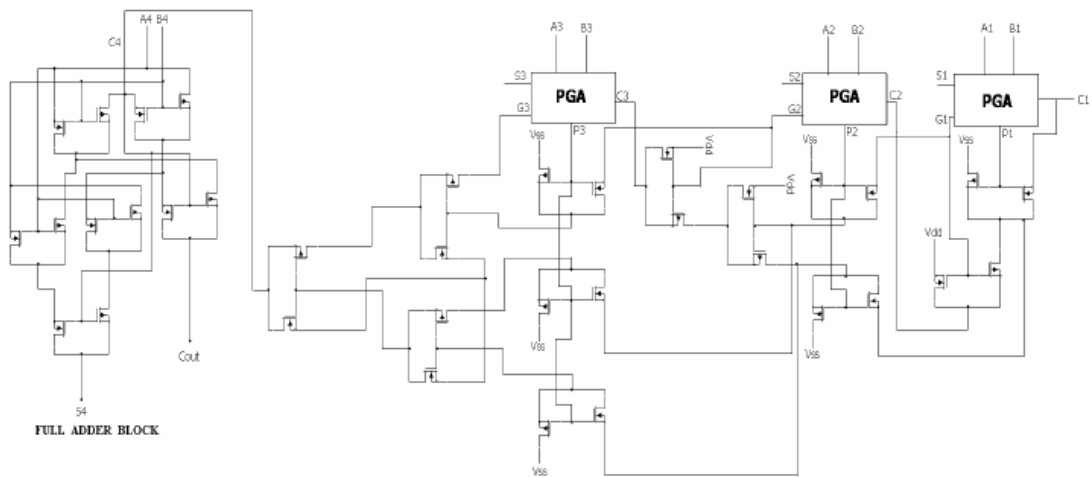


Figure 14. Transistor Implementation of NCLA using proposed AND and OR gates and Multiplexer based full adder

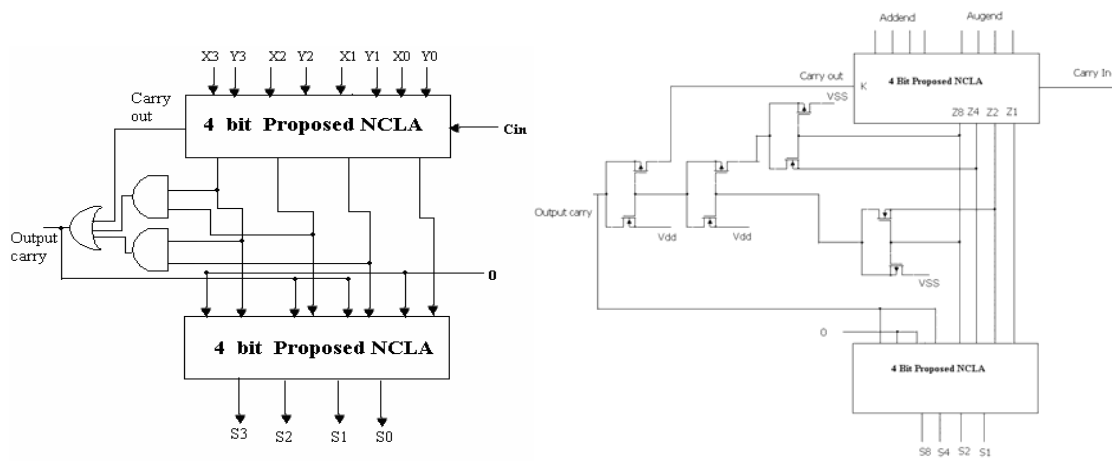


Figure 15. (a) Proposed CLA BCD Adder (b) Transistor implementation of the proposed CLA BCD adder