An Algorithm for Yield Improvement via Local Positioning and Resizing

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Abstract
The ability to improve the yield of integrated circuits through layout modification has been recognized and several techniques for yield enhanced routing and compaction have been developed. The approach described in this paper is aimed to improve the random defect limited yield of the VLSI design. The goal is achieved by increasing the design tolerance to short (extra material) and open (missing material) type defects. This approach and the suggested algorithm can be used as a post place and route step for improving catastrophic yield loss caused by the random defects.

Keywords
Yield, layout optimization, yield improvement.

INTRODUCTION

One of the major challenges facing semiconductor companies today is how to increase the yield. Since yield is directly related to profitability, an IC designer can significantly increase the income by predicting and improving yield before the tapeout. With the move to nanometer design and shrinking geometries further, the sensitivity of silicon to manufacturing defects has been increased.

There are three basic approaches that are used commonly for layout yield improvement. They are: the architectural choices that should be done before the physical design stage (like redundancy, etc), the layout modification during the process of physical design, and the reconfiguration technique, which is being done during the chip manufacturing process.

The idea of YI through layout modification is in decreasing the area which is sensitive to random defects - so called critical area, that way increasing the defect tolerance of the IC design. There are two basic techniques for improving the defect limited yield:

a. Wire spreading - by increasing the distance between routing geometries the layout becomes more tolerant to the short type defects.
b. Wire widening – by increasing the width of the geometries, they become more tolerant to open type defects.

The method described in this paper uses both these techniques simultaneously by choosing the optimal (in terms of yield) width and local placement of each of the wires during the pass. The approach is iterative, during each of the iterations either horizontal or vertical geometries are being processed. By controlling the number of iterations (as well as the order of directions) the optimal quality versus performance ratio can be reached.

The rest of the document is organized as follows: section 2 covers some details regarding the yield calculation models used in this work, section 3 contains the algorithm for finding the locally optimal placement and size of one wire, section 4 describes a possible flow using the approach and section 5 stands for the summary.

All the terminology and notation that are not defined but used here can be found in [1] and [2].

YIELD CALCULATION MODEL

Subsections

It will be assumed that the defect size density function (both for open and short defects) can be described by a power law (*pl*) for defects smaller than the critical size x_o and by an inverse power law (*ipl*) for defects larger than the critical size. Then,

a. The defect size density function for shorts $G_{short}(x)$ can be de fined by

$$G_{SHORT}(x) \approx \begin{cases} k1 * x^{pl}, & if \quad 0 \le x \le S_o \\ \begin{cases} \dfrac{k2}{x^{ipl}}, & if \quad S_o \le x \le S_M \\ 0 & otherwise \end{cases} & otherwise \end{cases}$$

Let's suppose that the minimal allowed distance between the design objects is greater than S_O, which is very close to the minimum spacing rule. Now if the smoothly natural extension of the function $G_{short}(x)$ can be defined after the point S_M, then we can use the following formula:

$$G_{SHORT}(x) \approx \frac{k2_{short}}{x^{ipl}}$$

b. The defect size density function for opens - $G_{open}(x)$

$$G_{OPEN}(x) \approx \begin{cases} k1_{open} * x^{pl}, & if \quad 0 \le x \le O_o \\ \begin{cases} \dfrac{k2_{open}}{x^{ipl}}, & if \quad O_o \le x \le O_M \\ 0 & otherwise \end{cases} & otherwise \end{cases}$$

can analogously be defined by the following function:

And again, supposing that the minimal allowed object size is greater than O_O, and if we after the point O_M take the smoothly natural extension of the function $G_{open}(x)$, then we can use:

$$G_{OPEN}(x) \approx \frac{k2_{open}}{x^{ipl}}$$

Open Fault Probability for Single Routing Geometry (rectangular)

Let's consider a pattern consisting of a single metal line of width W and length L. The critical area for open type defect of size D in this case should be defined by the following formula [1],

$$CA_{open}(x) \approx \begin{cases} (x-W)L + \frac{1}{2}(x-W)\sqrt{x^2 - W^2}, & if\ x \geq W \\ 0, & if\ x < W \end{cases}$$

Assuming $W<<L$, the critical area can be well estimated by a linear function of the defect diameter x, and will have the following form:

$$CA_{open}(x) \approx \begin{cases} (x-W)L, & if\ x \geq W \\ 0, & if\ x < W \end{cases}$$

Having this we can get the average number of faults (ANF) for open type defects using the formula [1].

$$ANF_{open}(W, L) = D^0_{open}\int_W^\infty CA(x)G_{open}(x)dx$$
$$= D^0_{open}L\int_W^\infty (x - W)G_{open}(x)dx$$

where $D^O{}_{open}$ is the average number of open type defects.

Short Fault Probability for Two Neighboring Routing Geometries (rectangular)

For a pair of wires with the common span L and the spacing S, the critical area is defined by this formula

$$CA_{short}(x) \approx \begin{cases} (x - S)L + \frac{1}{2}(x - S)\sqrt{x^2 - S^2}, & if\ \ x \geq S \\ 0, & if\ \ x < S \end{cases}$$

and again can safely be approximated by a linear function of the defect diameter x, which can be given by the following form:

$$CA_{short}(x) \approx \begin{cases} (x - S)L, & if\ \ x \geq S \\ 0, & if\ \ x < S \end{cases}$$

And, like in case of opens, the average number of faults for Shorts can be estimated by

$$ANF_{short}(S, L) = D^0_{short}\int_S^\infty CA(x)G_{short}(x)dx$$
$$= D^0_{short}L\int_W^\infty (x - S)G_{short}(x)dx$$

where $D^O{}_{short}$ is the average number of short type defects.

LOCALLY OPTIMAL POSITIONING AND SIZING OF ONE WIRE

Let us now start with some definitions. Let's assume we are in the vertical optimization iteration and denote the horizontal wire being processed by w. Let the functions $W = W(w)$ and $L = L(w)$ be the width and the length of the wire w. By the two sets of wires *{b1…bm}* and *{t1…tn}* we will denote the top and bottom neighboring geometries. The property "neighbor" is defined between two geometries, it is dependent on the direction and can be described as follows:

Definition 1: Geometries u and v are neighbors in vertical direction, if there can be drawn a vertical interval that crosses both these shapes and does not cross any other shape. The similar formulation can be given for the horizontal direction.

Definition 2: Let the term *span* stand for the length of the common projection of the neighboring geometries on the direction perpendicular to the optimization direction. Let us use the function *span(u,v)* for the span between vertices u and v.

Definition 3: Let us use the term *dist* for the minimal spacing between projections of two geometries on the optimization direction. Let us use the function *dist(u,v)* for the distance between vertices u and v.

Definition 4: Let us denote by distMin(x,y) the minimum allowed spacing between geometries x and v.

Then, lets denote by $ST=\{st_1,\ldots,st_n/st_n=span(w,\ t_j)\}$ and $SB=\{sb_1,\ldots,sb_n/sb_n=span(w,b_j)\}$ the set of spans with the top and bottom neighborhood of the wire w.

Let us also use $DT=\{dt_1,\ldots,dt_n/dt_n=dist(w,\ t_j)\}$ for distances between the top and $DB=\{db_1,\ldots,db_n/db_n=dist(w, b_j)\}$ bottom neighboring geometries and the wire w. Now the total ANF will be

$$ANF_{total} = ANF_{open}(W, L) + \sum_{i=1}^{n} ANF_{short}(st_i, L) + \sum_{i=1}^{m} ANF_{short}(sb_i, L)$$

where $L = \sum_{i=1}^{n} a_i$.

Now, considering each of the top and bottom edges of the wire w independently and letting them move freely across the optimization direction we can write the following formula:

$$ANF_{total}(u, v) = ANF_{open}(W + u + v, L) + \sum_{i=1}^{n} ANF_{short}(st_i - u, L) + \sum_{i=1}^{m} ANF_{short}(sb_i - v, L)$$

where u specifies how much the top edge of the wire w goes up and v – how much it's bottom edge goes down. The obvious aim of this yield optimization problem is the

minimization of the abovementioned function. Doing some simplifications we can write

$$ANF_{total}(u,v) = \frac{k2_{open} \cdot L \cdot D^0_{open}}{(2-3 \cdot iplo + iplo^2)}(W+u+v)^{2-iplo} + \sum_{i=0}^{n} st_i \cdot \frac{k2_{short} \cdot L \cdot D^0_{short}}{(2-3 \cdot ipls + ipls^2)}(dt_i - u)^{2-ipls} + \sum_{i=0}^{m} sb_i \cdot \frac{k2_{short} \cdot L \cdot D^0_{short}}{(2-3 \cdot ipls + ipls^2)}(db_i - v)^{2-ipls}$$

By doing the following replacement

$$Cns_{open} = \frac{k2_{open} \cdot L \cdot D^0_{open}}{(2-3 \cdot iplo + iplo^2)}$$

$$Cns_{short} = \frac{k2_{short} \cdot L \cdot D^0_{short}}{(2-3 \cdot ipls + ipls^2)}$$

we can get

$$ANF_{total}(u,v) = Cns_{open}(W+u+v)^{2-iplo} + \sum_{i=0}^{n} st_i \cdot Cns_{short} \cdot (dt_i - u)^{2-ipls} + \sum_{i=0}^{m} sb_i \cdot Cns_{short} \cdot (db_i - v)^{2-ipls}$$

It is known that the necessary condition for a function to reach it's extremum is the equality to zero for all the partial derivatives of first order of that function. It means

$$\partial_u ANF_{total}(u,v) = 0$$

and

$$\partial_u ANF_{total}(u,v) = 0$$

Now let's determine the domain of the function. We have the following assumptions:

a) $0 \le u + v$;
b) $u \le min_{i=1..n} \{st_i\}$ - $distMin(WM)$;
c) $v \le min_{i=1..n} \{sb_i\}$ - $distMin(WM)$;

where WM is the maximal allowed width for this wire. Then the domain region for the function should look like in the figure 1.

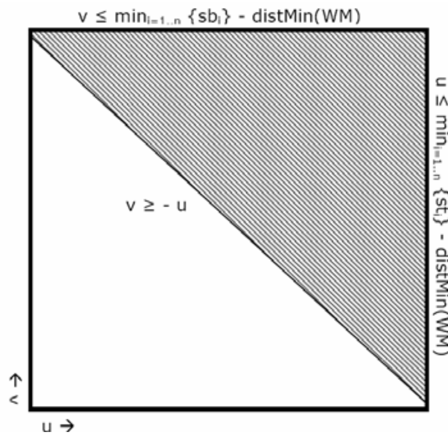

Figure 1. The domain of the function.

Now let's use Newton's method for solving this minimaztion problem. Please use [3] for the terminology and notation used below.

The problem can be stated as follows: Given the continuous functions $f(x,y)$ and $g(x,y)$, find the values $x=x^*$ and $y=y^*$ such that $f(x^*,y^*)=0$ and $g(x^*,y^*)=0$.

It means we need to solve a system of two nonlinear equations:

$$\begin{cases} f(x,y) = 0 \\ g(x,y) = 0 \end{cases}$$

assuming that an approximate solution to this set is known - (x_i, y_i). Using Newton's method we will need to solve the following equation set for calculation of the next point:

$$\begin{cases} f_x(x_i,y_i) \cdot \Delta x_i + f_y(x_i,y_i) \cdot \Delta y_i = f(x_i,y_i) \\ g_x(x_i,y_i) \cdot \Delta x_i + g_y(x_i,y_i) \cdot \Delta y_i = g(x_i,y_i) \end{cases}$$

where the next point can be found using this rule

$$\begin{cases} x_{i+1} = x_i + \Delta x_i \\ y_{i+1} = y_i + \Delta y_i \end{cases}$$

This is an iterative approach, so these two equations should be applied repetitively until either one or both of the following convergence criterias are satisfied:

a. $|\Delta y_i| \le \varepsilon_g$ and $|\Delta x_i| \le \varepsilon_f$

b. $|g(x_{i+1}, y_{i+1})| \le \varepsilon_g$ and $|f(x_{i+1}, y_{i+1})| \le \varepsilon_f$

where ε_f and ε_g are the approximation parameters for driving the iterative process and are passed by the user. For faster convergence in Newton's method the selection of the initial point is very important.

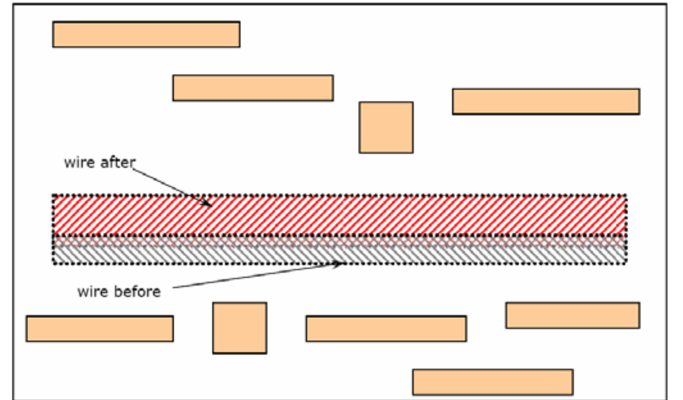

Figure 2. Result on a sample configuration.

A POSSIBLE YIELD OPTIMIZATION FLOW

Based on the proposed positioning and widening technique for one wire, a complete layout optimization flow can be constructed. One example of such a flow can be given by the following pseudocode.

INPUT:

ListOfDirections: the set of directions (horizontal or vertical) in which the spreading/widening should be done.

NumberOfIterations: the number of iterations that should be performed on each direction…

ListOfPrimaryWires: the set of wires that are applicable for the current direction of optimization.

ALGORITHM:

```
for_each_direction dir in ListOfDirections
{
  CollectApplicableWires(ListOfPrimaryWires)
  for iteration = 0 to NumberOfIteration
  {
     for_each_wire w in ListOfPrimaryWires
     {
        GetTopNeighborHood(w,topNeighbors)
        GetBottomNeighborHood(w,bottomNeighbors)
        ResizeAndlace(w,topNeighbors,bottomNeighbors)
     }
  }
}
```

OUTPUT:

The new location and width of all the routing geometries in the design layout.

SUMMARY

The biggest advantage of this approach is that it is based on the tradeoff between critical areas of short and open type defects. Besides, since it is iterative, changing the number of iterations one can also achieve the “effort level versus runtime” tradeoff.

Another advantage is in possible application to any IC layout during it’s physical implementation without changing the die size and increasing the yield by just doing minor modification on the layout, avoiding another iteration of the back-end flow.

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