Crosstalk at the Dynamic Node of Domino CMOS Circuits

Waleed K. Al-Assadi, Vipin Sharma, and Pavankumar Chandrasekhar
Department of Electrical and Computer Engineering, University of Missouri – Rolla
1870 Miner Circle, Rolla, MO 65409 U.S.A.
Email: {waleed, vsmq7, cphx5} @umr.edu

Abstract - The need for faster circuits in smaller area with lower power dissipation has made it a common practice to use the domino CMOS in high performance integrated circuits. However this improved performance comes at the cost of lower noise immunity. Also current trends in integrated circuit technology have increased chances of crosstalk due to capacitive coupling. Though several works have investigated the problem of crosstalk at the inputs of domino circuits, crosstalk at the dynamic node of the domino circuits has been ignored. A model for crosstalk at the dynamic node is developed and verified in this paper. Application of this model can ensure immunity of domino circuits from crosstalk failures.

Keywords: VLSI, Domino CMOS Circuits, capacitive coupling, crosstalk model, crosstalk noise, design for test.

1. Introduction

Domino CMOS circuits belong to the dynamic logic circuits family. Their operation is based on the storage of charge on a capacitive node and the conditional discharging of that node as a function of the inputs. The structure of a domino circuit is shown in Figure 1. C_L represents the capacitance of the node.

The circuit operates in two phases: precharge and evaluation. In the precharge phase CLK = 0. The dynamic node, D, is precharged to VDD through the PMOS precharge transistor and the output of the domino gate is set to 0. When CLK = 1, the circuit is in the evaluation phase

This work is supported by Missouri Research Board under grant No. R5003188.

The precharge transistor is off and the footer transistor is turned on. Depending on the input values and the pull-down topology, the dynamic node is conditionally discharged. If the pull-down network does not conduct, the precharged value remains stored in the capacitance of the dynamic node, C_L. If conditions are such, that the pull-down network conducts, a low resistance path exists between the dynamic node and GND and the dynamic node discharges to GND. Once the dynamic node is discharged it cannot be charged again till the next precharge phase. Therefore an input to the gate cannot make more than one transition during evaluation. The *keeper* transistor is a weak transistor whose purpose is to replenish charge lost due to charge leakage and charge sharing without affecting the functionality of the circuit [1].

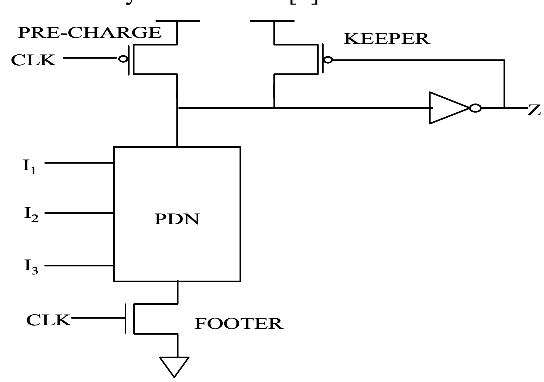

Figure 1: Domino CMOS gate

Domino CMOS circuits offer designers the advantages of higher speed, smaller area, and lower power dissipation than equivalent static circuits, but at the cost of lower noise immunity for the following three reasons.

Domino logic cannot recover if a noise pulse discharges the precharged dynamic node in the evaluation phase. Secondly, during the evaluation phase the pull-down network starts conducting as soon as the input exceeds the threshold voltage of the NMOS transistors. Therefore domino logic has a small noise margin. Finally, when the pull-down network is not conducting during evaluation, the dynamic node is in a high impedance state [2]. This makes the circuit very sensitive to crosstalk effects at the dynamic node. *Crosstalk* is the unwanted interference between signal lines in circuits. It occurs due to resistive, inductive or capacitive coupling between signal lines. Current trends in integrated circuit technology like the scaling down of device size in integrated circuits, faster switching speeds, more metal layers, mixing of devices with different driving capabilities in the same integrated circuits and greater levels of manufacturing variations have increased the potential of failures due to crosstalk and further reduced noise immunity of domino circuits.

Different aspects of the crosstalk problem have been addressed in previous works. For example, Kundu et al. presented a method to analyze domino circuits for susceptibility to crosstalk failures from a layout extracted netlist and identify sites in the circuit that may fail due to crosstalk [3]. They described a test pattern generation methodology that generates specific test patterns to target crosstalk failures while combining the effects of crosstalk, charge sharing and leakage [4]. They also presented a timed test generation methodology for domino circuits [5].

In [6] a crosstalk noise model specific to domino circuits is presented which takes the effect of the keeper into account and provides more accurate noise measure. Kim et al developed procedures to minimize the capacitive cross-coupling effects for domino logic circuits based on the concept of crosstalk immunity set [7]. In [8] models that specify the circuit noise immunity in terms of amplitude and duration of the noise pulse are developed. The works cited here consider crosstalk occurring at the circuit inputs but tend to overlook the fact that crosstalk can also occur in the dynamic node. Though the dynamic node is internal to the domino gate, it inter-connects at least five transistors (3 drain and 2 gate terminals). The metal shape forming the dynamic node is longer than other metal shapes connecting the internal nodes, thus increasing the chances of capacitive coupling and crosstalk at the dynamic node.

This paper is organized as follows. Section 2 introduces the problem of crosstalk noise at the dynamic node. Section 2.1 refines the expression derived for the equivalent peak voltage at the dynamic by including the effects of noise pulse width. The effects of primary input levels (Section 2.2) and velocity saturation phenomenon on crosstalk noise (Section 2.3) are briefly discussed. A crosstalk noise model is then derived in section 3 which expresses the circuit immunity in terms of switching speeds and coupling capacitance at the dynamic node. The model is validated using SPICE simulations in section 4.

2. Crosstalk at Dynamic Node

The extent of crosstalk between adjacent signal lines due to capacitive coupling is decided by three factors: the coupling capacitance between victim and aggressor, the switching speed (risetime or falltime) of the signal on the aggressor, the width of the noise pulse, input pattern dependence of noise immunity, and the resistance driving the victim line. Due to crosstalk an up (down) transition on the aggressor causes a rise (fall) in voltage on the victim [9]. This analysis examines the voltage variation induced in the dynamic node of a domino circuit caused by a voltage noise on a neighboring wire and capacitive coupling between the two. Qualitative analysis of spurious transitions coupled from the gate of the precharge device to the drain (or dynamic node) due to the gate-drain capacitance is also presented.

Consider a metal inter-connect (line 1) which is capacitively coupled to the dynamic node (node 2) of a domino circuit by a coupling capacitance C_{12} as shown in Figure 2. Assume that inputs are such that the dynamic node is being driven to GND through the pull-down network.

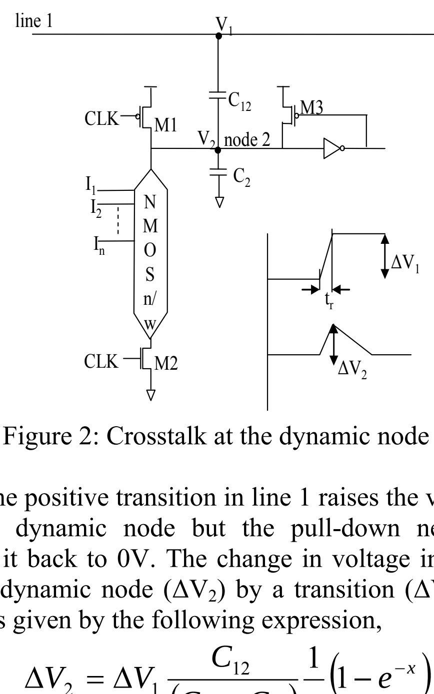

Figure 2: Crosstalk at the dynamic node

The positive transition in line 1 raises the voltage of the dynamic node but the pull-down network drives it back to 0V. The change in voltage induced at the dynamic node (ΔV_2) by a transition (ΔV_1) on line1 is given by the following expression,

$$\Delta V_2 = \Delta V_1 \frac{C_{12}}{\left(C_{12} + C_2\right)} \frac{1}{x}\left(1 - e^{-x}\right) \quad (1)$$

where $x = \dfrac{t_r}{R \cdot \left(C_{12} + C_2\right)}$

Similarly a falling edge on line 1 induces a drop in voltage at the dynamic node. t_r is the time the aggressor signal takes while switching for ΔV_1 amplitude. C_2 is the storage capacitance of the dynamic node and is composed of the diffusion capacitances of the precharge, discharge and keeper transistors, the gate capacitance of the output inverter and the wire capacitance. R is the equivalent resistance of the device(s) that is (are) driving the dynamic node. There are three possible values for R representing the three possible failure modes:

Mode 1: The precharge phase of operation of the circuit where R is the on resistance of the precharge transistor M1 in parallel with the ON resistance of the keeper (M3). Although the keeper transistor is very weak, it is expected to strengthen its driving abilities due to continued scaling of technologies [10]. This is because continued scaling of technologies is causing the leakage current to become more and more part of the normal driving currents. This is necessitating a stronger keeper presence relative to the other device's (pre-charge and PDN) strengths.

Mode 2: The evaluation phase, with the NMOS network is conducting, where R is the equivalent resistance of the NMOS network and the footer transistor (M2).

Mode 3: During the evaluation phase with the NMOS network not conducting, where R is the on resistance of the keeper transistor (M3).

If the circuit is in the conditions described in modes 1 and 3 above, the dynamic node is at V_{DD} and the circuit output is at logic 0. In such circumstances a falling edge on line 1can drop the voltage at the dynamic node to below V_{IL} of the output inverter and change the circuit output to logic 1.

In mode 1 the precharge transistor is always conducting, therefore the dynamic node can return to V_{DD} and the circuit may able to recover from the failure. In mode 3, once the output switches from logic 0 to logic 1 the keeper stops conducting, the dynamic node is no longer being driven by any device and the output remains at logic 1 Similarly, the circuit fails if a rising edge occurs on the aggressor with the domino circuit in conditions described in case 2 above.

In case 2 the dynamic node has discharged to 0 V, but if crosstalk raises its voltage to V_{IH} of the output inverter, the output of the circuit changes erroneously from logic 1 to logic 0. This error also may be temporary since the pull-down network can drive the dynamic node back to 0 V.

2.1 Analysis of the Noise Pulse

In the crosstalk analysis so far it was assumed that if the dynamic node voltage reaches below V_{IL} due to 1→0 noise pulse on the aggressor node, the output static inverter will switch erroneously from 0→1. This however is pessimistic estimation of the lower limit of the boundary condition. To better estimate the drop in the dynamic node voltage required for the static inverter to switch erroneously, it is necessary to consider the width of the noise pulse. Two conditions should be met for the static inverter to switch erroneously: The dynamic node voltage should drop down to V_{IL} or below and it should remain below V_{IL} for at least W_{MIN} of the time where W_{MIN} is given by [8]:

$$W_{MIN} = \Delta t_{(sat)} + \Delta t_{(lin)} \qquad (2)$$

where $\Delta t_{(sat)}$ is the time for which the PMOS transistor in the static inverter is in the saturation region and $\Delta t_{(lin)}$ is the time for which the PMOS transistor in the static inverter is in the linear region. W_{MIN} is expressed in terms of static inverter's parameters [8] as given by equation 3. This means the dynamic node voltage has to drop V_w more below V_{IL} of the static inverter. Following illustrates the derivation of V_W.

$$W_{MIN} = \frac{C_{out}}{\beta(\Delta V_2 + V_{tp})^2}(V_{DD} + V_{IH} - \Delta V_2 - V_{tp}) \qquad (3)$$

Two cases can be considered: (1) The aggressor noise pulse width (W_N) is greater than W_{MIN} and (2) the aggressor noise pulse width is less than or equal to W_{MIN}.

Case (1): Figure 3 illustrates the case when the noise pulse width is greater than W_{MIN} of static inverter. The keeper transistor helps pulling the dynamic node up after the dynamic node's noise voltage reaches its minimum peak.

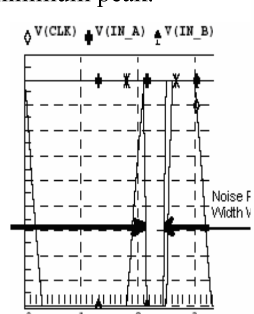

Figure 3(a).
Noise Pulse

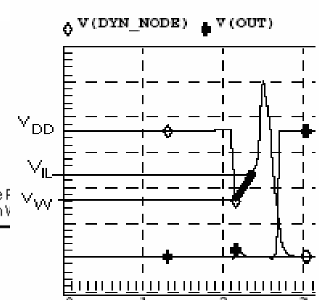

Figure 3(b).
Noise at Dynamic node

The aim is to derive the magnitude of V_W which specifies how much below V_{IL} the dynamic node has to be pulled down and stay below V_{IL} in order for the static inverter to switch erroneously.

At the boundary condition, this duration (as shown by bold line in Figure 5 (b)) is used by keeper to pull the node up. Assuming the noise pulse has a peak to peak switch of VDD→0 value, an equivalent model for the keeper pulling the node is shown in Figure 4. As can be seen, the equivalent capacitance for the keeper is $C_2 + C_{12}$ which it drives up through R_{ON} keeper resistance.

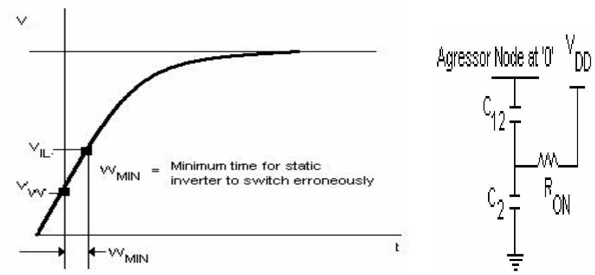

Figure 4: Equivalent circuit of keeper pulling the dynamic node up

The expression for V_W can be derived by a simple methodology involving the charging equation of dynamic node capacitor through the linear region resistor (R_{ON}) of the keeper. This is illustrated by Figure 4. V_W is given by following expression:

$$V_W = \frac{V_{IL}}{V_{DD}} - \left\{ 1 - e^{-\left[\frac{W_{MIN}}{R_{ON}(C_2 + C_{12})}\right]} \right\} \qquad (4)$$

It should be noted that for the static inverter to switch ON erroneously, V_W should be always greater than or equal to '0'. A negative value of V_W implies the impossibility of the static inverter to switch erroneously with the given R_{ON} and W_{MIN} values. This is an important result against an analysis employing only the rise time of the noise pulse and ignoring the pulse width information.

Case 2: For the case in which the width of the noise pulse W_N is less than the W_{MIN} of the static inverter, an analysis of similar kind as in case 1 can be done to derive V_W. It is easily seen that if the rise time of the noise pulse (t_{RN}) is less than the speed with which the keeper transistor pulls the dynamic node up, V_W is given by the same expression as given by equation 4.

However if the rise time of the noise pulse is less than pulling up speed of the keeper, a slightly different strategy can be employed as illustrated by Figure 5.

Figure 5 shows the shape of noise on dynamic node if $W_N < W_{MIN}$. V_W can be derived by knowing the rise time of noise pulse (t_{RN}) and charging equation of the dynamic node capacitance through keeper resistance. It is to be noted that keeper charges the dynamic node during W_N and the rest of pulling up time of the dynamic node is contributed by the noise pulse itself. With these findings it is easy to derive V_W as given by following expression:

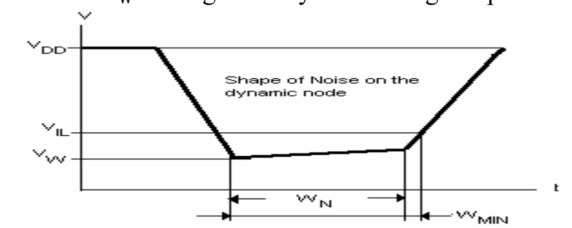

Figure 5: Zoomed view of the shape of noise on dynamic node for $W_{MIN} > W_N$.

$$V_W = \frac{V_{IL} - V_{IL}'}{V_{DD}} - \left\{ 1 - e^{-\left[\frac{W_{MIN}}{R_{ON}(C_2 + C_{12})}\right]} \right\} \qquad (5)$$

Where $V_{IL}' = \frac{0.8 V_{DD} (W_{MIN} - W_N)}{t_{RN}}$

For the case of rising noise pulse on the dynamic node, derivation of V_W will be similar to the derivation discussed earlier with the exception that this time the dynamic node pulse has to rise till V_W.

2.2 Effects of Primary Input Levels on the Crosstalk Noise

The crosstalk analysis done ignores the changes in the primary inputs levels of the dynamic circuit. Although changes in the primary input levels are statistical and hence difficult to predict, there effects can vary significantly on the crosstalk model derived above. The effects (positive and negative) get more pronounced as the pull down network (PDN) encompasses more number of NMOS transistors.

Figure 6 shows a simple AND dynamic circuit. Ca is the internal node capacitance of Ma and Mb NMOS transistors while A & B are the primary inputs. Consider now the evaluation phase of the circuit. Assume input 'A' stays at logic 1 and 'B' makes a transition from 0 → 1 after some time of the beginning of the evaluation phase. Since NMOS transistor Ma turns ON the dynamic node capacitance can be approximated as Ca + C_2 neglecting R_{ON} of Ma NMOS transistor. This decreases the contribution of C_{12} in the overall capacitance thus increasing the overall noise immunity of the circuit as demonstrated in the HSPICE simulations later in Figure 8. The noise immunity can significantly increase if contribution of internal capacitance to the dynamic node capacitance is considerable.

HSPICE simulation was done for validation with typical values as: Ca = 3.5fF, C_2 = 15fF V_{DD} = 1.8 volts and fall (V_{DD} →0) time of aggressor line = 1.0 ns.

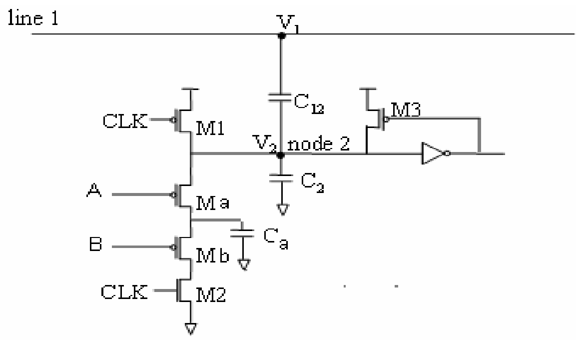

Figure 6: A Simple Dynamic AND Gate

Figure 7 shows the HSPICE simulations for this simple circuit for two conditions: 1) When transistor Ma is ON throughout the evaluation period while Mb switches ON after some time of the beginning of the evaluation period. 2) When transistor Mb is ON throughout the evaluation period while Ma switches ON after some time of the beginning of the evaluation period. The value of the dynamic node capacitance (C_2) was chosen such that any value less than this value will cause the dynamic node voltage value to fall down to static invertor's V_{IL} causing a spurious 0→1 transition at the output node.

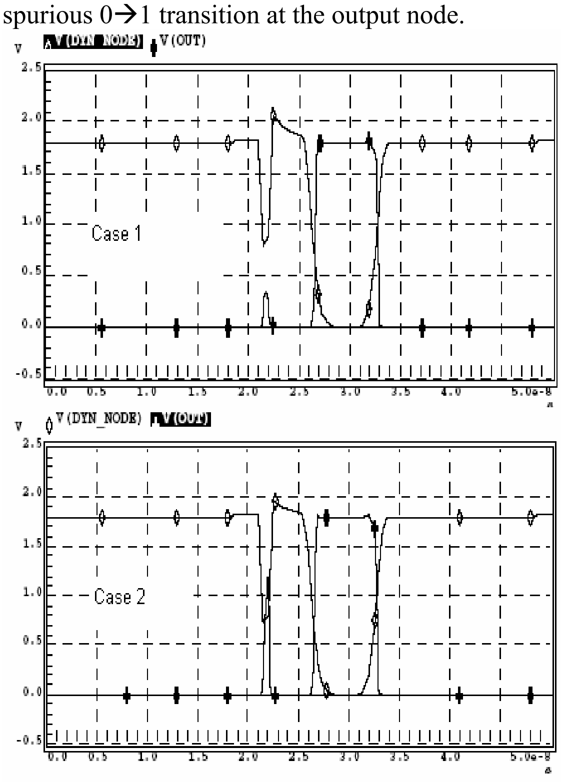

Figure 7: Spice demonstration of effects of primary input levels on crosstalk noise

As can be seen in Figure 7, transistor Ma remaining ON throughout the evaluation period is beneficial to the noise immunity of the design.

Case I thus shows that the noise pulse of same width is incapable of pulling down the dynamic node voltage below V_{IL} of the static inverter. Case II in contrast has spurious output transition from 0→1 since the internal capacitance of the internal node did not contribute to the total dynamic node capacitance. This suggests that for crosstalk analysis the inclusion of effective internal node capacitance to the dynamic node capacitance of a dynamic gate will yield precise results provided we have pre-knowledge of input patterns in certain circuits like counters, etc.

2.3 Crosstalk Noise at CLK Net

It is necessary to examine any spurious transitions on gate of the precharge transistor (CLK) through gate-to-drain (C_{GD}) parasitic capacitance since it is very closely comparable to the dynamic node capacitance.

For a simple AND dynamic circuit shown previously, the gate-to-drain capacitance of precharge transistor was estimated to be 1 fF to 7 fF. 7fF of C_{GD} is just half of the dynamic node capacitance and can be a dominant factor for transferring any spurious transitions on the CLK net (gate of precharge transistor) to the high impedance dynamic node. This capacitance is, however, variable which depends on the driving strength of the precharge transistor. The driving strength (V_{GS} – Vtp) of the precharge transistor is very low in the evaluation period and hence C_{GD} of the precharge transistor is negligible. Thus any effect of spurious transitions on the CLK net cannot be propagated to the dynamic node in the evaluation mode. Noise transitions on the CLK net can thus be ignored as the impact on the dynamic circuit's noise immunity is very less.

3. Crosstalk Noise Model

Knowing V_W, V_{IL} and V_{IH} of the output inverter and using expression (1) it is possible to specify the circuit noise immunity in terms of the voltage transition on line 1 (ΔV_1) and the coupling capacitance (C_{12}) for each of the three modes.

For modes 1 and 3 where the dynamic node is being driven by the precharge and keeper transistors respectively, the condition for noise immunity is given by

$$\Delta V_1 \frac{C_{12}}{(C)} \frac{1}{x}\left(1 - e^{-x}\right) \leq V_{DD} - V_W \qquad (6)$$

where $C = C_{12} + C_2$

Using the e^x expansion and equating the two sides of equation (6) we can derive the safe minimum fall (rise) times of the aggressor switching with ΔV_1 amplitude which includes the effects of width of the noise pulse.

$$t_f = \frac{3}{2} R(C)\left[1 - \sqrt{\left(\frac{8}{3} \cdot \frac{C}{C_2} \cdot \frac{(V_{DD} - V_W)}{\Delta V_1}\right) - \frac{5}{3}}\right] \quad (7)$$

For the case where the pull-down network is conducting

$$t_r = \frac{3}{2} R(C)\left[1 - \sqrt{\left(\frac{8}{3} \cdot \frac{C}{C_2} \cdot \frac{V_W}{\Delta V_1}\right) - \frac{5}{3}}\right] \quad (8)$$

Expressions 7 and 8 give the minimum falltime and risetime of the signal on the aggressor switching with ΔV_1 amplitude that will not cause crosstalk failure. These expressions include the effects of width of the noise pulse. If width of the noise pulse is not known, an approximation for these minimum times can be derived by ignoring V_W. These expressions which do not consider noise pulse width information are given by equations 9 and 10 below:

$$t_f = \frac{3}{2} R(C)\left[1 - \sqrt{\left(\frac{8}{3} \cdot \frac{C}{C_2} \cdot \frac{(V_{DD} - V_{IL})}{\Delta V_1}\right) - \frac{5}{3}}\right] \quad (9)$$

$$t_r = \frac{3}{2} R(C)\left[1 - \sqrt{\left(\frac{8}{3} \cdot \frac{C}{C_2} \cdot \frac{V_{IH}}{\Delta V_1}\right) - \frac{5}{3}}\right] \quad (10)$$

On the other hand if the circuit designers know the switching speed of signals on the aggressor, these expressions give the maximum coupling capacitance (C_{12}) that will not cause crosstalk. This information can be used to identify potential crosstalk failures sites in circuit layout or it can be used to design crosstalk resistant circuit layout.

Substituting typical values of R, C_2, ΔV_1 and V_{IL} in 5.7, the plot of t_f versus C_{12} is shown in Figure 8. The noise immunity curve divides the graph into a safe and unsafe region. For example in the case of pulse width consideration, if the coupling capacitance is 35 fF the minimum safe fall time of a signal on the aggressor is 210 ps. On the other hand, ignoring the width of the noise pulse gives the minimum safe fall time of the aggressor signal as 500 ps. Thus the crosstalk analysis including the pulse width gives a better estimate of the minimum fall time.

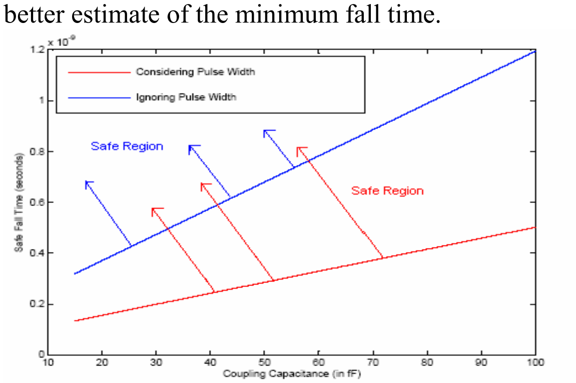

Figure 8: Safe/Unsafe fall times against a given value of decoupling capacitance.

It should be noted that the curves start from 15 fF of the decoupling capacitance axis since any value less than 15 fF cannot pull the dynamic node down below V_{IL} of the static inverter and hence there is no possibility of any erroneous switching. Thus the entire vertical region on the left of 15 fF decoupling capacitance is a safe region.

The actual (10-90%) rise time (Tr) & fall time (Tf) of the aggressor signal is different from that given by equation 10 and 9 respectively if ΔV_1 is not equal to $|V_{DD}|$ and can easily be derived.

$$T_r = \frac{0.8\, t_r}{\Delta V_1} V_{DD} \quad \text{and} \quad T_f = \frac{0.8\, t_f}{\Delta V_1} V_{DD} \quad (11)$$

4. SPICE Validation

The proposed crosstalk model was verified by SPICE simulations. The victim circuit designed for the simulations implemented the function

$$Z = A.B + B.C + A.C \quad (13)$$

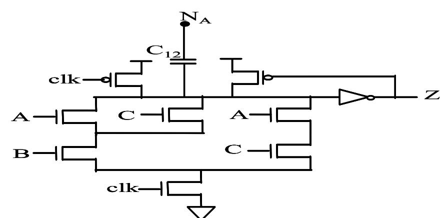

Figure 9. Test circuit for SPICE validation

The diffusion capacitances of the precharge, discharge and keeper transistors and the gate capacitances of the transistors in the output inverter were calculated using the transistor dimensions and process parameters. C_2 was found as 15.897 fF. Using the transistor dimensions and process parameters and by considering the transistors to be in the linear mode of operation, the resistance driving the dynamic node (R_{ON} equations 7 and 8) was calculated for the evaluation mode where keeper pulls the dynamic node up after a noise pulse. Rail to rail swing was assumed in the aggressor node i.e. $\Delta V_1 = V_{DD} = 1.8$ V. After simulating crosstalk failure in the test circuit, the calculated and observed values of switching speeds were compared.

The domino circuit is most vulnerable when it is being driven by the keeper in the evaluation phase. The keeper is a weak device and has a high on resistance of 160.24 kΩ. Figure 10 compares the simulated and calculated values of falltimes that cause crosstalk. It can be seen that increasing the value of coupling capacitance between the aggressor node and the dynamic node the minimum safe fall time of the noise pulse increases. Also including the minimum pulse width requirements shows close results with SPICE simulations.

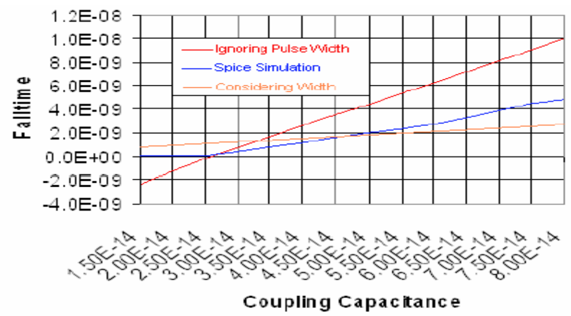

Figure 10. Crosstalk during evaluation

5. Conclusion

A study of the three cases reveals the following facts. For lower values of coupling capacitance the calculated values of rise/fall times required to cause crosstalk are negative. In real circuits rise/fall times cannot be negative. In simulations of such low values of coupling capacitance even transitions of zero rise/fall times do not cause crosstalk. This indicates that the model was lacking required information which was fulfilled by considering the effects of minimum pulse width required for the output static inverter to switch ON erroneously.

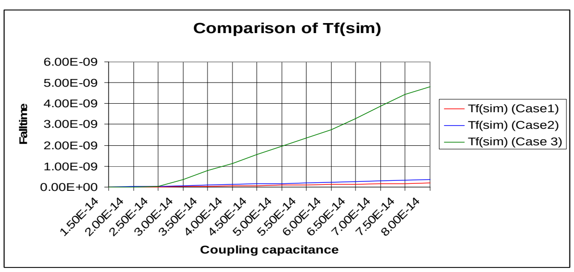

Figure 11. Comparison of three failure modes

Rise and fall times of typical CMOS circuits are of the order of a few tenths of nano-seconds. It was observed that at these switching speeds, in all three cases the calculated crosstalk immunity curve was always included in the "safe" region of the simulated crosstalk immunity curve when minimum pulse width required were not taken into consideration. Therefore by using the newly proposed crosstalk model which considers the effects of minimum pulse width requirements very close approximations of the realistic noise immunity specifications can be derived with high accuracy. On comparing the crosstalk immunity curves of the three failure modes and judging the accuracy of the model with minimum pulse width requirements, it was found that the circuit was most vulnerable in the case where the circuit is in the evaluation phase with the pull-down network not conducting. This was valid for the calculated and the simulated crosstalk immunity curves. The reason for this is the high resistance of the keeper that is driving the dynamic node. Figure 11 compares the simulated crosstalk immunity curves for the three failure modes. It shows that the safe operating region is basically decided by the third case (i.e. the evaluation phase with pull-down network not conducting). Therefore this case should be given highest priority when designing the circuit.

6. References

[1] Waleed K. Al-Assadi, Pavankumar Chandrasekhar, Bonita Bhaskaran, "Fault Modeling and Testability of CMOS Domino Circuits", *Proceedings of the 2005 International Conference of Computer Design*, pp. 21-27, June 27-30, 2005.

[2] J. M. Rabaey, A. Chandrakasan, B. Nikolic, "Digital Integrated Circuits, A Design Perspective", pp. 284-294, 2nd edition 2004.

[3] R. Kundu, R.D. Blanton, "Identification of crosstalk switch failures in domino CMOS circuits," *Proc. Intl. Test Conference,* pp. 502-509, October 2000.

[4] R. Kundu, R.D. Blanton, "ATPG for noise-induced switch failures in domino logic," Intl. Conf. on Computer Aided Design (ICCAD 2003), pp. 765-768, November 2003.

[5] R. Kundu, R.D. Blanton, "Timed test generation for crosstalk switch failures in domino CMOS," *Proc. 20th IEEE VLSI Test Symposium (VTS 2002),* pp. 379-385, April 2002.

[6] S. H. Choi, K. Roy, 'A new crosstalk noise model for DOMINO logic circuits," *Conf. and Exhibition on Design, Automation and Test in Europe*, pp. 1112-1113, 2003.

[7] K-W. Kim, S-M. Kang, "Crosstalk noise minimization in domino logic design," *IEEE Trans. On Computer Aided Design of Integrated Circuits and Systems,* vol. 20, no. 9, pp. 1091-1100, September 2001.

[8] A. Kabbani, A. J. Al-Khalili, "A technique for dynamic CMOS noise immunity evaluation," *IEEE Trans. On Circuits and Systems I: Fundamental Theory and Applications,* vol. 50, no. 1, pp. 74-88, January 2003.

[9] Li Ding, Pinaki Muzumder, "On Circuit Techniques to Improve Noise Immunity of CMOS Dynamic Logic", *IEEE Trans. On Very Large Scale Integration (VLSI) Systems,* vol. 12, no. 9, September 2004.

[10] Ki-Wook Kim, Sung-Mo Kang, "Crosstalk Noise Minimization in Domino Logic Design", *IEEE Trans. On Computer-Aided Design of Integrated Circuits and Systems,* vol.20, no.9, September 2001.