

# Design of low power 4-tap 8-bit adiabatic FIR filter

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**Abstract**— Digital signal processing (DSP) is used to perform filtering, decimation and down conversion in common communications systems, like in oversampling analog to digital converters in wireless and audio applications. This paper describes a design of low order FIR (finite impulse response) filters to be used at the high sampling rates for achieving a low power DSP implementation. This paper reviews the asymptotic zero energy dissipation techniques named as Adiabatic switching logic. The Adiabatic switching technique beats the dynamic power as well as short circuit power, using recycling of energy stored on circuit capacitances instead of dissipating it as heat. PAL technique is the simplest fully adiabatic technique requiring lesser number of power clocks as well as area. Design of four tap 8-bit fully pipelined FIR filter, using PAL adiabatic technique and CMOS technique is compared at different operating frequencies from 5 MHz to 100 MHz, the range which includes input sampling rate for GSM (10 MS/s) and DECT (50 MS/s) standards. Comparison also includes the power loss in adiabatic power supply. Using 0.25  $\mu\text{m}$  technology and 3.3 V voltage supply, energy saving in PAL compared to CMOS is 3 times to 15 times, with frequency varied from 100MHz down to 5MHz.

## I. INTRODUCTION

DSP is used in almost all the communications systems, for example in decimation filter in sigma-delta analog to digital converters, low and high frequency filtering of digital signals, down sampling etc. Energy dissipation of CMOS circuits is becoming a major concern in the design of DSP systems. Currently the power consumption of CMOS circuits drops linearly with operating frequency. This means that energy consumption per cycle is constant. The reason for the high dynamic dissipation of conventional CMOS is the fact that charge transfer within them happens abruptly. Usually time constant is much larger than  $RC$  of the circuit, so idea of adiabatic is to spread the transitions over the whole cycle to reduce the energy consumption. Adiabatic circuits should satisfy two conditions: First, charge flow between two nodes in the circuit occurs in a gradual and externally controlled manner, which implicitly means that the device should never be turned on if there is potential difference across it and never be turned off if significant current is flowing through it. Second, charge path should not contain any non-linear dissipative elements like diode[1][2][3].

To illustrate the advantage of adiabatic techniques [4], using the model shown in Fig. 1 for energy analysis of CMOS

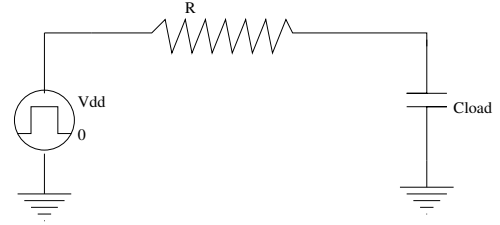


Fig. 1. Energy analysis model of CMOS circuits

circuits, energy dissipation is given by

$$E_{dynamic} = -\frac{V_{dd}^2}{R} \int_0^{\infty} e^{-2t/RC} dt = \frac{CV_{dd}^2}{2} \quad (1)$$

The dynamic dissipation in CMOS is not an irreducible minimum associated with charging and discharging a capacitive node. Charging a node to  $V_{dd}$  from 0 in a period  $T$ , requires a current  $i(t)$  such that

$$\int_0^T i(t) dt = Q = CV_{dd} \quad (2)$$

But energy dissipation is related to current by

$$E = R \int_0^T i^2(t) dt \quad (3)$$

Therefore, current function  $i(t)$  should be such that the Eq. 3 could be minimized while obeying constraint posed by Eq. 2. Such a current function is given by

$$i(t) = Q/T = CV_{dd}/T \quad (4)$$

So step voltage source should be replaced by the constant current source (ramp voltage source). The resulting model will be called as adiabatic circuit model in which energy dissipation will be inversely proportional to the charging time of ramp i.e. power dissipation has quadratic dependence on the frequency given by equation Eq. 5.

$$E_{ramp} = CV_{dd}^2 \times \frac{2RC}{T} \quad (5)$$

The number of partially and fully adiabatic logic families are available[5] till date. In the second section, fully adiabatic families Split-Level Charge Recovery Logic(SCRL)[1][4] and

pass transistor adiabatic logic(PAL)[6] are reviewed and compared with justification to the selection of PAL to use it in our FIR filter design with adiabatic technique, which needs only two clocks to implement any combinational and sequential design.

Third section includes the design of 4-tap fully pipelined adiabatic FIR Filter using booth-multiplier and carry-lookahead-adder having latency of 24 cycles and throughput of 2 samples per cycle. The design and schematic of basic cells for building multiplier and adder using PAL technique and there sizing issues are discussed. Which is compared with pipelined CMOS FIR Filter using same basic components and having latency of 16 cycles and throughput of 1 samples per cycle.

Next section describes the topology used for the design of power supply for adiabatic circuits[7]. Power supply design for adiabatic circuits is very much complex than that of CMOS. The architecture used to implement this topology which consist of differential ring oscillator and asynchronous finite state machine is described.

Last section compare the simulation results of adiabatic and conventional FIR filters from power dissipation point of view at different operating frequencies, which also includes losses in the power supply, using 0.25  $\mu\text{m}$  technology which is most important for wireless LAN applications. And in such applications where voltage supply is agreed to be 3.3 V.

## II. FULLY ADIABATIC LOGIC TECHNIQUES

Fully adiabatic logic always have lower power dissipation than partial adiabatic logic and standard CMOS logic for frequencies whose upper limit is decided to reduce the inrush flow of current. Because in standard CMOS circuits discharged node is connected to constant DC supply or charged node to GND voltage at the time of evaluation, which is like node is charged with step voltage having infinite switching frequency. And in partial adiabatic logic some of the nodes in the circuit are charged with constant voltage supply while some with the power clock(ramp voltage), so overall there will be more power dissipation than the fully adiabatic logic. In this section, fully adiabatic logic techniques which will lead to reduce power dissipation compared to standard CMOS logic are reviewed.

Fully adiabatic circuits available till date are split-level charge recovery logic(SCRL)[1][4], 2-level adiabatic logic(2LAL)[8], pass transistor adiabatic logic(PAL)[6], true single phase energy recovery logic(TSEL)[9] and single phase source coupled logic(SPSC)[9][10][11]. In SCRL and 2LAL, energy stored at any node is recovered by next reversible stage. As shown in Fig. 2, SCRL inverter is identical to conventional inverter except for addition of pass gate with its control clocks  $P1$  and  $/P1$  and top and bottom rails  $\phi1$  and  $/\phi1$  driven by clock instead of  $V_{dd}$  and  $GND$ . Top rail swings from  $V_{dd}/2$  to  $V_{dd}$  and bottom rail swing from  $V_{dd}/2$  to  $0$  during evaluation phase and in the reverse direction during restoring phase. The problem in SCRL technique is that the last stage of pipeline could not be reversible, but irreversible dissipation in last

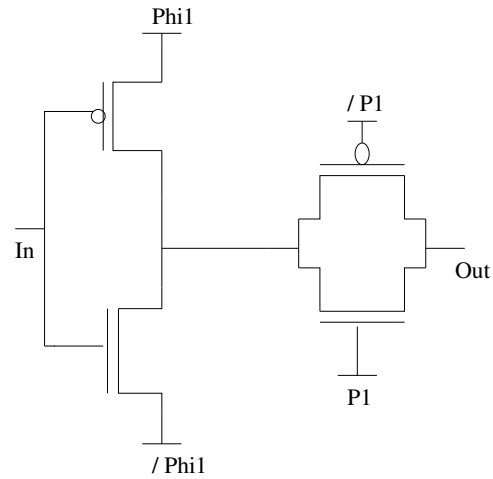


Fig. 2. SCRL inverter

stage is negligible for long pipelines. The second problem with SCRL is requirement of 4 to 36 number of clocks for different-phase of timing for pipelining, which makes this technique to be not used in practice or very difficult to implement. The third problem is double the area required by this technique, which increases the capacitance and hence power dissipation because of quadratic dependence of power on capacitance of the circuit.

The 2LAL is the logic having cross coupled T-gates as basic buffer element[8]. It needs four timing signals(power clocks) with 4 ticks per cycle. Area required to implement this logic is also large, as an example it needs 4 T-gates to implement buffer requiring 8 transistors. Here also, every next stage is consist of forward block for data flow and reverse block to recycle the energy from output node of previous stage, which increases the area by 2 times and also need each logic implementation to be reversible. Charge from last stage of pipeline could not be recovered adiabatically.

TSEL, SPSC and PAL are the logic where same logic stage do charging as well as recovery of the charge from its output node. The TSEL logic[9] which is further modified to SPSC logic[10][11] is a true single phase logic operational with only single power clock, requires DC biasing and hence will have more power dissipation in the circuit. Here circuit nodes are also charged non-adiabatically for some part of the power clock cycle, due to which these are less efficient than PAL for frequencies less than 40 MHz. These logics also require more number of transistors: one transistor to provide biasing and two more to switch the nodes from non-adiabatic charging to adiabatic charging for each logic stage, demanding more area.

PAL is a dual rail logic with relatively low gate complexity: a PAL gate consists of true and complementary NMOS functional blocks, and a pair of cross coupled PMOS devices  $Q1$  and  $Q2$  as illustrated by example of Fig. 3. The PAL gate is supplied by a sinusoidal power clock PC.

The PAL fully adiabatic family is chosen for designing FIR filter because it overcomes all the problems incurred in SCRL fully adiabatic family: (a) Last stage of the pipeline is also

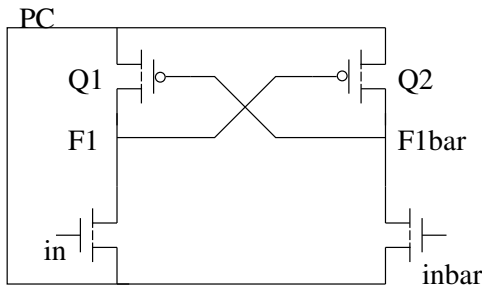


Fig. 3. PAL inverter

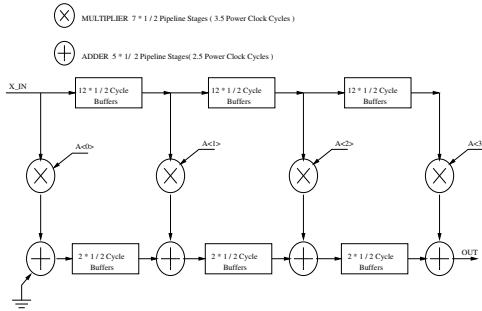


Fig. 4. Block Diagram of PAL-FIR filter

reversible and hence there will be ease in designing, because circuit comprising of thousands of pipeline circuits will never suffer from dissipation at the end of pipeline, (b) Requires only two clocks which are complement of each other (c) It uses pass transistor implementation hence thereby reducing the capacitance, and dual rail implementation results in easy non-inverting implementation and hence further reduction in capacitance. This technique is more efficient than TSEL and SPSC for the desired frequency range which includes input sampling rate for GSM (10 MS/s) and DECT (50 MS/s) standards.

### III. DESIGN OF FULLY ADIABATIC AND NON-ADIABATIC FIR FILTER

PAL technique and conventional CMOS techniques are used to design 4-tap pipelined FIR filter using booth-multiplier [12], carry-look-ahead adder[12], buffer as the basic cells. Booth encoding a multiplier input halves the number of partial products reducing delay and area in both array and tree-based multipliers, hence reduces the power dissipation at the architectural level. Pipelining is free in the PAL topology as it does not need any flip flop to pipeline the combinational blocks. Fig. 4 shows the block diagram of 4-tap adiabatic FIR filter, which is basically a Direct-Form-II architecture[13], in which major change is the inclusion of buffers in the upper line to equalize the delay of multiplier and adder for every tap. Since multiplier needed 5-pipelined PAL stages and adder needed 7-pipelined PAL stages, one stage is evaluated in one-half of the power clock cycle, so total of 6 clock cycles delay is implemented using 12 PAL-buffer in series for each of the tap. Since this is very deep pipeline implementation, so latency

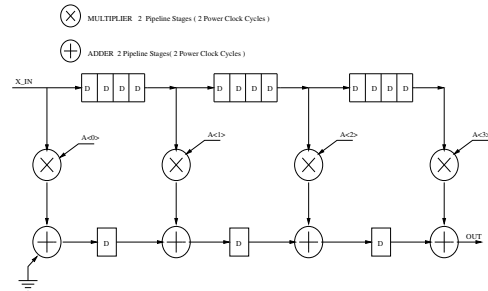


Fig. 5. Block Diagram of CMOS-FIR filter

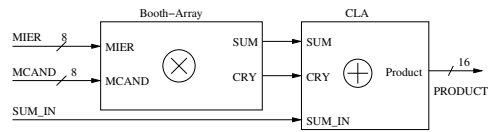


Fig. 6. Block Diagram of booth multiplier

is very high (24 cycles) but throughput is 2 samples/cycle. Since it is the necessity in the PAL technique to pipeline the circuit at the gate level, these circuits should be used in the DSP application where large latency is not a big problem. But parallelism can also be used to reduce the latency very efficiently.

Similarly for the CMOS technique Fig. 5, booth-multiplier and CLA each is divided into two stages of equal delays, resulting in 4-stage pipelined logic. This delay is equalized by 4 D-Flip-flops in the upper line for each of the tap resulting into FIR filter having latency of 16 cycles and throughput of 1 sample/cycle.

Booth radix-4 multiplier is designed to reduce the delay by decreasing the number of partial products and hence adders. Booth multiplier examines three bits of the multiplicand at a time to determine whether to add 0, 1\*, -1\*, 2\* or -2\* of that rank of the multiplicand. These operations are performed using three control signals: ZERO zeroes the operand, NEG inverts the operand and TWO multiplies the value by 2(left shift) generated by two current bits of multiplicand and the previous bit. It is divided into two parts as shown in Fig. 6 one the booth-array and other a carry-lookahead-adder. The booth-arrays accepts two 8-bit inputs, MIER<7:0>(the multiplier) and MCAND<7:0>(the multiplicand) and feeds the CLA. The CLA also accepts a 16-bit input(SUM-IN<15:0>), which is used to perform multiple-accumulates.

As shown in Fig. 7, It consists of 4 ranks of adders each 9-bit wide. The first rank degenerates to schematic shown in Fig. 8 and remaining ranks are represented by the schematic in Fig. 9. Both ranks use a booth decode cell which is shown in Fig. 10. This cell observes 3 bits of MIER and produces the control signals X1, X2 and N<1:0> which are used in the array adders shown by Fig. 8 and 9. From Fig. 8, the first rank is fed by MIER<1:0> and Vss, 2nd rank is fed by MIER<3:1> and so on, to determine the control signals and the partial products. Each rank retires two bits of the partial product sum(SUM) and carry(CRY) so by the last adder rank

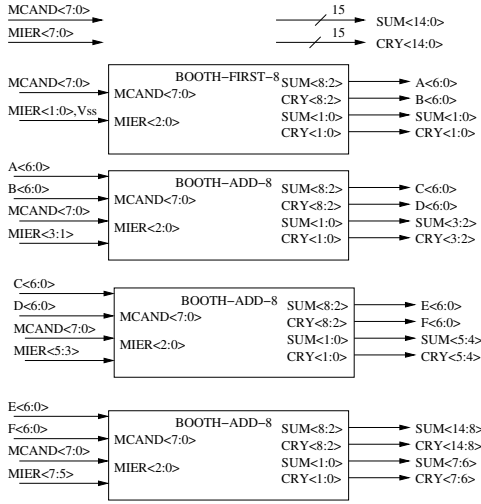


Fig. 7. Detailed Diagram of booth array

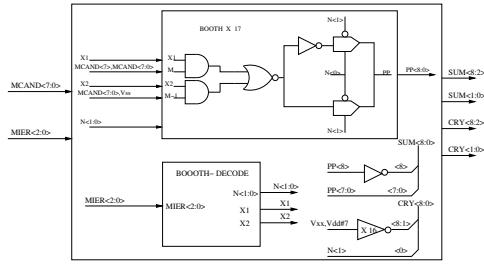


Fig. 8. Detailed Diagram of 1st rank of booth array

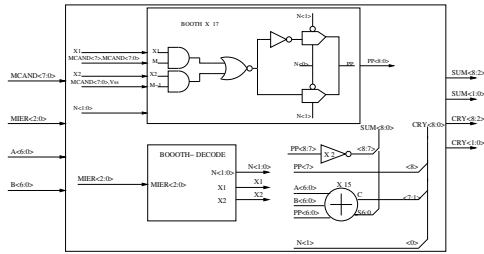


Fig. 9. Detailed Diagram of rest of the ranks of booth array

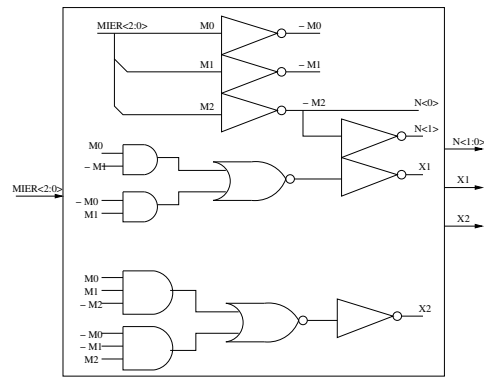


Fig. 10. Detailed Diagram of booth-decoder to generate control signals

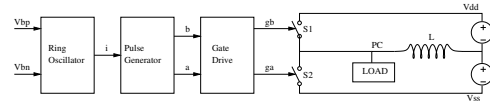


Fig. 11. Block Diagram of Power Supply

15 SUM, CRY pairs have been produced. These are used by the CLA to produce a 16-bit result. Next each of the rank consists of a booth decode, 9 booth gates and a 9-bit carry save adder.

At each rank the SUM shifts right by two bit positions while the cry shifts right by one bit position. Finally, SUM and CRY results of booth-multiplier and SUM-IN from the previous tap are added using CLA.

#### IV. DESIGN OF POWER SUPPLY

The adiabatic power supply needs an efficient energy recovery design which implies quality factor  $Q$  of the power supply to be very high. Not only the  $Q$  should be high, it should be proportional to cycle time so that energy dissipation in the power supply should also decrease with frequency. Otherwise, dissipation in the power supply itself will dominate the logic circuit dissipation at lower frequencies. Mostly preferable technique is to use sinusoidal voltage supply because of its ease to design as compared to pure trapezoidal wave. In inductor based approach [4] energy can be circulated between electrostatic field in the load capacitor and magnetic field in the off-chip inductor. Analysis of this approach [4] shows that by applying sinusoidal ramp, energy saved in the circuit is reduced by the factor of  $\pi^2/8$  compared to pure trapezoidal wave. And total energy consumption including the power supply is given by

$$E_{sinusoidal} = C_L V_{dd}^2 \left( \pi \sqrt{\frac{\tau_s}{T}} + \frac{\pi^2 \tau_c}{8T} \right) \quad (6)$$

where  $\tau_c$  and  $\tau_s$  are the time constants of circuit branches of computing part and supply part of the system respectively.

Zero-voltage switching push pull power conversion topology[7] is well suited for driving the large capacitive loads, as the peak current conducted by the main power switches is much smaller than the peak inductor current. The resulting power switches are thus small, with small conduction losses and small gate-drive dissipation. Design is composed of a ring oscillator which feeds a clock signal to a pulse generator as shown in Fig. 11. The pulse generator alternates gate pulses to control the main power switches S1 and S2. These switches conduct current to and from an external inductor, adding energy to the inductor in a controlled manner from two external DC supplies, which also supply  $V_{dd}$  and  $V_{ss}$  to the adiabatic circuitry. Switches S1 and S2 are switched-ON in an alternating fashion, pumping the resonant LC system with energy derived from the supplies. This energy is added at the maximum and minimum power-clock voltage, so that the switches are turned on when the blocking voltage is nearly zero. The amount of current conducted by the switches is related to the energy required by the system to maintain a

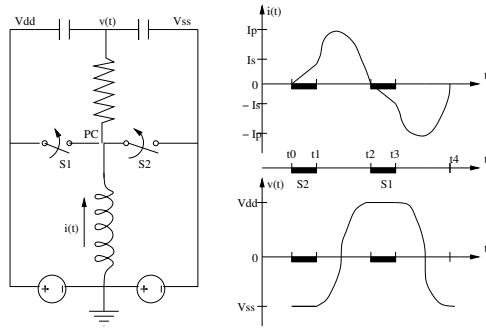


Fig. 12. Topology of Power Supply

stable power-clock amplitude. For typical adiabatic loads, this current is much less than the peak current flowing through the inductor into the load capacitance.

### V. SIMULATION RESULTS

Simulations are performed using  $0.25\mu$  technology and 3.3 V voltage supply (with which most of the communication systems are designed). Tool used for simulations is Analog Design Environment of Cadence. First, basic cells like buffer, gates, full-adder, half-adder, partial product generator are developed and then they are used in design of booth-multiplier, carry-lookahead-adder with appropriate sizing. Finally booth multiplier and carry lookahead adder are used to design FIR filter according to the structures shown in Fig. 4 and Fig. 5. Simulated result of 8-bit booth multiplier, 8-bit carry-lookahead-adder, 8-bit 4-tap FIR filter using PAL technique and conventional CMOS technique are shown in Table I.

TABLE I  
POWER DISSIPATION ( $\mu$ W) WITH PAL ADIABATIC TECHNIQUE AND CMOS TECHNIQUE

| Frequency (MHz) | Blocks    | 5      | 25     | 40     | 80    | 100   |
|-----------------|-----------|--------|--------|--------|-------|-------|
| CLA             | Adiabatic | 6.266  | 55.486 | 149.52 | 404   | 668   |
|                 | CMOS      | 50     | 252    | 402    | 805   | 1010  |
| MUL             | Adiabatic | 19.304 | 188.44 | 467.76 | 1408  | 2138  |
|                 | CMOS      | 287    | 1440   | 2300   | 4600  | 5800  |
| FIR             | Adiabatic | 77.48  | 754    | 1874   | 5640  | 8568  |
|                 | CMOS      | 1160   | 5800   | 9300   | 18510 | 23340 |

The above results include power dissipation of adiabatic supply. The clock input to the conventional CMOS technique is externally applied. Plots in Fig. 13, Fig. 14 and Fig. 15 shows the observations of power consumption per cycle of different blocks for different frequencies with PAL and CMOS techniques respectively.

Energy saving in PAL compared to CMOS is 2 to 8 times in carry-lookahead-adder, 3 to 15 times in booth-multiplier and FIR-filter, with frequency varying from 100MHz down to 5MHz.

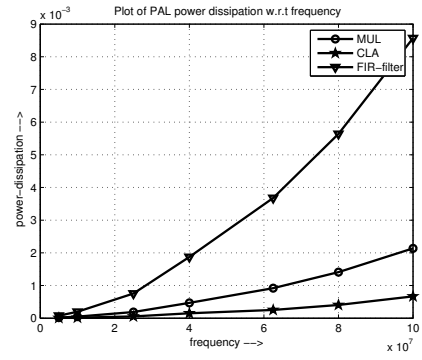


Fig. 13. Plot of power dissipation in PAL adiabatic case

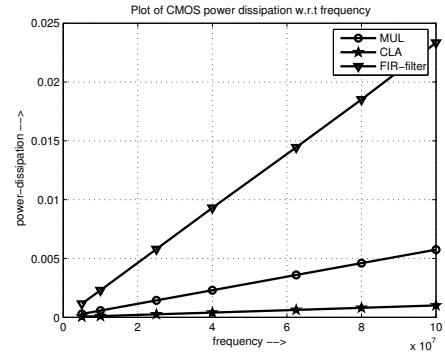


Fig. 14. Plot of power dissipation in CMOS case

### VI. CONCLUSION

All the fully adiabatic logic families are reviewed and PAL logic family is found to be best suited for DSP systems due to its low power performance in the frequency range of most of the communication systems, specifically includes input sampling rate for GSM (10 MS/s) and DECT (50 MS/s) standards. Its very promising properties w.r.t other logic families like only two power clocks, reduced area requirements, no termination of last stage of pipeline by non-reversible logic prove it to be economic and feasible. Moreover, circuits using this family are very easy to design because every next stage is powered by alternative clock, due to which each stage can be individually optimized while keeping the size of NMOS block fixed and

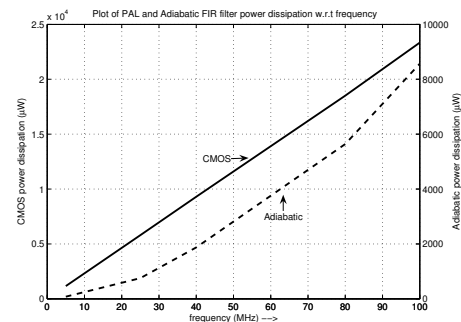


Fig. 15. Plot of power dissipation for FIR filter

size of back to back PMOS transistors can be optimized for driving the next stage as fast as possible without loading the previous stage.

The simulation results of FIR filter using PAL fully adiabatic technique and standard CMOS technique shows that PAL has large power saving at lower frequencies (15 times at 5 MHz frequency) and appreciable at higher frequencies (2 times at 100 MHz) compared to standard CMOS circuits.

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#### REFERENCES

- [1] Saed G. Younis, *Asymptotically Zero Energy Computing Using Split-Level Charge Recovery Logic*, Cambridge, MA, USA: Massachusetts Institute of Technology, 1994.
- [2] Saed G. Younis and Thomas F. Knight, *Practical implementation of charge recovering asymptotically zero power CMOS*, Proceeding of the 1993 symposium on Research on integrated systems, Cambridge, MA, USA: MIT Press, 1993.
- [3] Michael P. Frank, *Common Mistakes in Adiabatic Logic Design and How to Avoid Them.*, Embedded Systems and Applications, pages 216-222: DBLP, <http://dblp.uni-trier.de>, 2003.
- [4] Saed G. Younis, *Asymptotically Zero Energy Computing Using Split-Level Charge Recovery Logic*, Phdthesis, 1994.
- [5] Micah C. Knapp and Peter J. Kindlmann and Marios C. Papaefthymiou, *Design and Evaluation of Adiabatic Arithmetic Units*, Analog Integr. Circuits Signal Process, Hingham, MA, USA: Kluwer Academic Publishers, 1997.
- [6] Vojin G. Oklobdzija, Dragon Maksimovic, Fengcheng Lin, *Pass-Transistor Adiabatic Logic Using Single Power-Clock Supply*, IEEE Transactions On Circuits And Systems-II: Analog And Digital Signal Processing, Vol. 44, 1997.
- [7] Conrad H. Ziesler and Suhwan Kim and Marios Papaefthymiou, *A resonant clock generator for single-phase adiabatic systems*, ISLPED '01: Proceedings of the 2001 international symposium on Low power electronics and design, New York, NY, USA: ACM Press, 2001.
- [8] Ben Gojman, Nikil Mehta, Mary Pack, Eric Rachlin, and Dom Rizzo, *Reducing Power Dissipation in the Sublithographic Crossbar Architecture*, Robert Figueiredo: MIT EECS, 2004.
- [9] S Kim, MC Papaefthymiou, *True single-phase adiabatic circuitry*, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS, VOL. 9, NO. 1, 2001.
- [10] S Kim, MC Papaefthymiou, *Single-phase source-coupled adiabatic logic*, ISLPED '99: Proceedings of the 1999 international symposium on Low power electronics and design, pages 97-99, New York, NY, USA: ACM press, 1999.
- [11] S Kim, CH Ziesler, MC Papaefthymiou, *A True Single-Phase Energy-Recovery Multiplier*, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION SYSTEMS, VOL. 11, NO. 2, 2003.
- [12] Neil H. E. Weste and Kamran Eshraghian, *Principles of CMOS VLSI design: a systems perspective*, Boston, MA, USA: Addison-Wesley, 1985.
- [13] J.G. Proakis, D.G. Manolakis, *Digital Signal Processing*, New Jersey: Prentice Hall, 1996.