

# Shield effect analysis for a gate array on an Optically Reconfigurable Gate Array

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**Abstract**—To date, some types of Optically Reconfigurable Gate Arrays (ORGAs) have been developed to realize capabilities of rapid reconfiguration with numerous reconfiguration contexts. However, the layout style requires a shield against the reconfiguration light irradiation to guard transistors that constitute the gate array. This paper presents a shield effect for a circuit that is implemented on a gate array. Finally, experimental results are shown for an ORGA-VLSI chip with the shield design.

## I. INTRODUCTION

Recently, some types of Optically Reconfigurable Gate Arrays (ORGAs) have been developed to realize a larger gate count VLSI than that of conventional VLSI circuits, which use an optical memory [1]-[5]. These devices can have numerous reconfiguration contexts stored in a holographic memory and can quickly change the context on a gate array by reading the holographic memory.

The first ORGA had only an 80 gate count VLSI, 50–100 reconfiguration contexts in a holographic memory, a 16 to 20  $\mu$ s reconfiguration capability, and a total virtual gate count of 4,000–8,000 [1]-[3]. The reconfiguration speed was insufficient for clock-by-clock reconfiguration and the gate count of VLSI was very small.

The two demerits of slow reconfiguration speed and VLSI's small gate count in previously proposed ORGAs [1]-[3] result from the architecture, which includes a serial transfer circuit between photodiode array and gate array and double memory function for both sides. Therefore, we have introduced an improved uniformly distributed photodiode layout style in which each optical reconfiguration circuit is implemented close to a programming point of the gate array, thereby removing the serial transfers and double memory function. Results show that nanosecond-order reconfiguration capability and a real gate count of over 10,000 can be realized [4]-[5].

However, the new layout style requires a shield to guard transistors that constitute the gate array from reconfiguration light irradiation because transistors and photodiodes are separated only by a small distance. This paper presents a shield effect for a circuit implemented on a gate array. Finally, the experimental result of an ORGA-VLSI chip with the shield design is also shown.

## II. OPTICAL RECONFIGURATION CIRCUIT AND SHIELD DESIGN

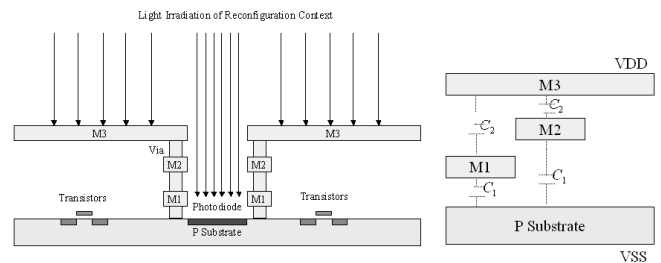


Fig. 1. Shield structure and parasitic capacitance of M1 and M2 layers.

The photodiodes are always constructed between N+ diffusion or N-WELL and a P-substrate as shown in Fig. 1. The photodiode perimeter is always surrounded by P+ diffusion with contacts connected to the first metal with ground potential. In addition, the other metal layers are mounted on the first metal layer, which is connected through vias to the ground potential. These rings act as shielding against the irradiation light. In addition, all transistors are protected from reconfiguration light irradiation using the top metal layer, which has only a hole on photodiodes and perfectly covers the other area. Therefore, metal layers aside from the top metal layer are used for wiring. However, the shield method engenders the following demerit: each metal line has capacitance not only to the P-substrate, but also to the top metal layer. The increased parasitic capacitance effect cannot be neglected. Therefore, the shield effect for metal wiring is discussed from the perspective of the frequency of a circuit implemented on a gate array. Calculating the difference between a non-shield and shield, Here, each capacitance is represented as the following equation.

$$T_{Shield}/T_{NonShield} = \frac{C_1 + C_2}{C_1}. \quad (1)$$

Here, each capacitance is represented as the following equation.

$$C = \epsilon_{ox}\epsilon_o \frac{w}{d} l. \quad (2)$$

In that equation,  $\epsilon_{ox}$  and  $\epsilon_o$  are the electric constant and a specific inductive capacity,  $w$ ,  $l$ , and  $d$  respectively denote the width, length of wire, and the distance between layers. Equation (1) can be rewritten as the following.

$$T_{Shield}/T_{NonShield} = 1 + \frac{d_2}{d_1}, \quad (3)$$

where  $d_1$  and  $d_2$  are the distance from a target layer to the substrate and to the top metal layer, respectively. Here,  $T_{Shield}/T_{NonShield}$  of the first metal layer and the second metal layer are defined as  $T_1$  and  $T_2$ , respectively. Also, the length of wire of the first metal layer and the second metal layer are defined as  $L_1$  and  $L_2$ , respectively. Using merely total metal wiring length of each metal layer, the total affection from a shield is expressed as following equation:

$$\Delta = \frac{ALL_{Shield}}{ALL_{NonShield}} = \frac{T_1L_1 + T_2L_2}{L_1 + L_2}. \quad (4)$$

Here, the transistor delay and wire delay of non-shield gate array are defined respectively as  $D_{Tr}$ ,  $D_{wire}$ . Using them, the total circuit delay  $T_{NonShield}$  of a non-shield gate array is expressed as

$$T_{NonShield} = D_{Tr} + D_{wire}. \quad (5)$$

Since the shield affects only the wire delay, the total circuit delay  $T_{Shield}$  of a shield gate array is calculated as

$$T_{Shield} = D_{Tr} + \Delta D_{wire}. \quad (6)$$

This is the analysis equation of a shield effect.

### III. EXPERIMENTAL RESULTS

A shield effect was analyzed using HSPICE simulation. A sample chip was designed using 0.35  $\mu\text{m}$  three-metal CMOS process technology. The result is shown in Table 1. A 2-bit adder and a 2-bit multiplier were implemented onto the designed ORGA to estimate the delay caused by adding a shield. The table shows the estimation result of three types: a gate array neglecting the metal interconnect delay; a gate array without the top metal layer shield; and a gate array with the top metal layer shield. The HSPICE simulation results show that the increasing delay caused by the top metal layer shield was only 7.1% – 9.5%, which is very small.

In addition, results of theoretical analysis using Eq. (6) show that the delays caused by the top metal layer shield were 13.0% – 13.5%. The result of theoretical analysis nearly equals the results obtained by the HSPICE simulation. This shield analysis is useful as a rough analysis of ORGA design before fabrication. The result also shows that the increasing delay effect is very small in 0.35  $\mu\text{m}$  CMOS process technology.

TABLE I  
TRANSITION TIME FROM 10% TO 90%.

Method / Circuit Type	2bit Adder	2bit Multiplier
Tr. Delay neglecting metal effects	7.0 [ns]	7.0 [ns]
Non-Shield Delay	8.5 [ns]	8.4 [ns]
Shield Delay	9.1 [ns] $\Delta$ 7.1%	9.2 [ns] $\Delta$ 9.5%

### IV. CONCLUSION

High-speed reconfiguration ORGAs requires a shield of the top metal layer to guard the gate-array transistors from reconfiguration light irradiation. Therefore, the shield effect for a circuit implemented on a gate array was analyzed using HSPICE simulation. In the case of using a 0.35  $\mu\text{m}$  three-metal CMOS process technology, the increased delays of a 2-bit adder and a 2-bit multiplier caused by the top metal layer shield were confirmed as less than 7.1% – 9.5%. In addition, results of theoretical analysis showed that the delays caused by the top metal layer shield were 13.0% – 13.5%. The result of theoretical analysis nearly equaled the results obtained by the HSPICE simulation.

The shield effect was confirmed as slight and the effectiveness of a uniformly distributed photodiode layout style for ORGAs was confirmed.

### V. ACKNOWLEDGMENT

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