ERSA'06

ENGINEERING OF RECONFIGURABLE SYSTEMS AND ALGORITHMS

This is the sixth conference on Engineering of Reconfigurable Systems and Algorithms (ERSA'06). It was founded in 2001 and, since then, has been held each year in the end of June in Las Vegas.

The configurable computing has gained more and more attention during last years. New promising application areas have replaced the traditional use of reconfigurable computing platform on FPGAs in prototyping and developing embedded systems. New applications together with new technology emphasise new problems to be solved. The new emerging areas are mobile handheld appliances (handheld computing and communication systems); mobile vehicular systems (automotive industry with computing and communication systems); supercomputing applications and configurable multiprocessors. During last years, the security related problems using configurable computing platform has gained particular interest.

ERSA conference solicits papers from all aspects of reconfigurable computing, including classical programmable logic, as well as configurable multiprogramming related papers. The topics of interests include theory, architecture, algorithms, design systems and applications that demonstrate the benefits of reconfigurable computing.

I would like to thank the authors for submitting their papers to ERSA'06 and for preparing the final versions of their papers for due date. I hope you all will have successful and enjoyable meeting in Las Vegas this year and I hope to meet you again in next years.

I would like to extend my deepest gratitude for the efforts extended by the ERSA'06 Program Committee and to all external reviewers for their careful reading of all of the submitted papers.

Last but not least, I would like to thank the organizing team of The 2006 World Congress in Computer Science, Computer Engineering, and Applied Computing, and, especially, the General Chair Prof. Hamid Arabnia, for the continuous support and help in organizing the ERSA conference.

Toomas P. Plaks
ERSA Chairman
London
May, 2006

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Welcome Message from ERSA Chair

The world is changing. The advances in microelectronics are changing the technology. One die can contain several billion transistors. This makes it possible, if not inevitable, to map into one die several processor cores. Also, the microelectronics market is changing. There is estimation that in the near future, in 2010, about 90are mobile, wireless consumer appliances that must be small in size, with very low power consumption and with high performance.

This will emerge changes in the design concepts of microelectronic devices, the design concepts of application-specific processors, as well as general-purpose processors. Many companies and researchers believe that the challenge for future is to use reconfigurablilty and parallelism, introducing configurable multiprocessing on a single die. The reconfiguring is migrating from the circuit level to the level of algorithms, while hundreds, if not thousands, simple processor-cores are replacing complex processors on a single die.

Configurable parallel processing has many advantages. First, it replaces time-consuming digital design by programming of multiprocessors reducing, thus, the design cost and time, and, makes the design reprogrammable. Second, algorithms are mapped directly onto configurable space of simple processors achieving the efficiency of Application-Specific Integrated Circuits (ASICs). Third, the multiprocessor concept facilitates the building of energy efficient systems using dynamic shutdown of unused processors. And last, the performance is scalable and depends on the algorithmic design, on the number of processors involved and not on the clock frequency of electrical circuits.

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