

VLSI Design of Multiple Specifications Viterbi Decoder

Chun-Guan Kim, HongMoon Wang, Dae-Jin Bae, and Jong Tae Kim^{*},

School of Information and Communication Engineering, Sungkyunkwan University,
300 Cheoncheon-dong, Suwon, Gyeonggi-do 440-746, South Korea

Abstract - In wireless communication, the channel state changes repeatedly. In this situation, we select the specification of the Viterbi decoder for the worst case channel state. However, if we select the specification of the Viterbi decoder with such a criterion, the decoder operates inefficiently in the good channel state. In this paper, we propose a specification controllable Viterbi decoder without using adaptive T-algorithm. This decoder provides 21 different specifications and can change its specification dynamically depending on the channel state.

Keywords : Viterbi decoder, channel state, specification control

1. Introduction

The Viterbi decoder operates using current and past input data. Because the Viterbi decoder has a simple architecture and fast decoding time, it has been widely used in the area of wireless communication.^[1] However, the existing Viterbi decoder architecture has a significant deficiency in the wireless communication environment, namely the repeated changes in the wireless channel state. Therefore, we select the specification of the Viterbi decoder for the worst case channel state in order to ensure a stable BER(Bit Error Rate). However, as a result, the Viterbi decoder operates inefficiently in the good channel state while providing better performance than is really necessary.^[2] Therefore, a Viterbi decoder architecture is needed in which the decoding performance can be controlled according to the channel state variation.^{[3],[4],[5]}

R.Henning and C.Chakrabarti simulated the variation of the viterbi decoder performance (using adaptive

^{*} Corresponding author

T-algorithm) which is changed by path metric threshold and truncation length according to the channel's E_b/N_0 .^[6] Also, Russel Tessier and Sriram Swaminathan confirmed the performance of adaptive Viterbi decoder architecture with T-algorithm. It was implemented with FPGA.^[7]

In this paper, we propose a specification controllable Viterbi decoder architecture without adaptive T-algorithm. The proposed architecture is implemented and verified with simulation using matlab and modelsim simulator.

2. Multiple Specification Viterbi decoder architecture

Figure 1 shows a block diagram of the multiple specification Viterbi decoder architecture. It basically operates in a continuous manner. The reconfiguration of the decoding depth is possible at any time. However, the reconfigure request signal (Reconfig_req) must be used for the reconfiguration of the constraint length. If Reconfigure request signal occurs, data input of BMC block is stopped and reconfig request signal (Reconfig_req_sig) is transferred to Systolic-array by Control-block. Control block is on standby until Systolic-array finishes their work with entered data. When entered data is completely decoded, Systolic-array transfers decode finish signal (Decode_finish_sig) to Control-block. Finally, Control-block sets new Viterbi decoder specification and generates reconfigure-finish-signal (Reconfig_ark).

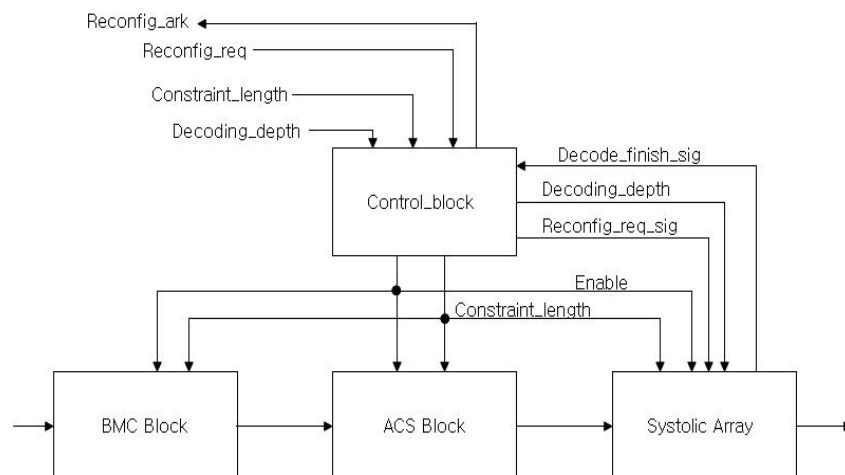


Fig. 1 Multiple spec. Viterbi decoder block diagram

2.1 BMC & ACS block architecture

Figure 2 shows a block structure diagram of the BMC and ACS. The *codeword store* block is a memory that stores the codeword data for each constraint length. Based on constraint length, codeword set is selected.

The structure of ACS block is almost the same as the existing one. However, path matrix calculation block, finding survival path block, and minimum path decision block are divided to several groups according to constraint length and they can operate respectively. In the result, the input of the unused block has a constant value in order to reduce switching activities.

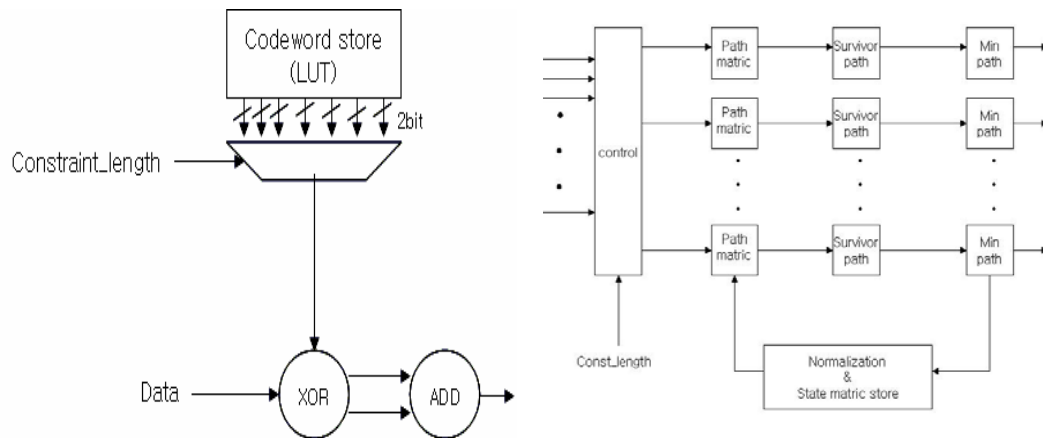


Fig. 2 BMC & ACS block structure diagram

2.2 Systolic Array Architecture

The systolic array has two types of component, as shown in figure 3. The difference between the two types is that type2 has *Load_out* and *Final_out* port but the other does not. The structure of the type2 is only used at the end stage of the systolic array. The *Load_out* signal is transmitted to the systolic array control block when the input data is assigned. Using this signal, the systolic array control block is made aware of the state of the data decoding operations. The *Final_output* port is the data out port. In the systolic array, the total number of type2 components is sixteen. According to the constraint length and decoding depth, Systolic array control block select one *final_output* data for the output of the Viterbi decoder among the sixteen possible values. When decoding depth is changed, systolic control operates two different ways according to difference between current decoding depth and next decoding depth. If new decoding depth is shorter than before, the output data is stored at shift register during the difference

of decoding depth clock cycle, and then drive out the data to decoder output port. If new decoding depth is longer than before, there are two different ways. First, shift register's MSB is driven out to decoder output port during the difference of decoding depth clock cycle if shift register is not empty. Second, Valid_out signal is driven to '0' to notify that output value is not valid if shift register is empty.

The reset signal for each component is controlled separately. Therefore, we can reduce the amount of unnecessary switching due to the existence of unused blocks.

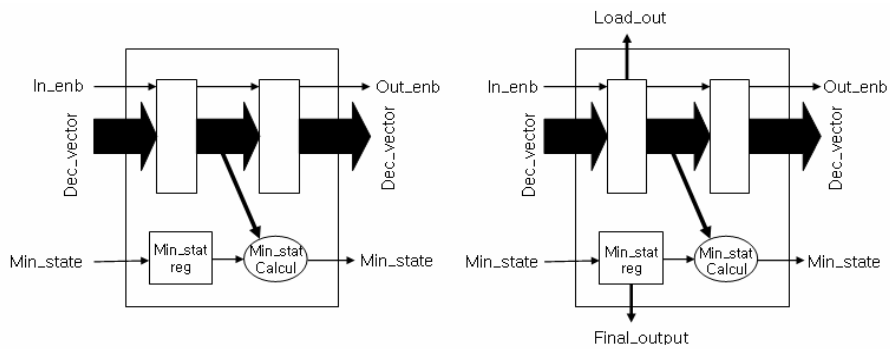


Fig. 3 Component of Systolic array structure (Left : type1, Right : type2)

3. Simulation

3.1 Synthesis Report

Table 1 represents synthesis report of the multiple specification Viterbi decoder. The area overhead of the implemented multiple specification Viterbi decoder is 16% more of that of the fixed specification Viterbi decoder (constraint : 9, soft decision bit : 4, decoding depth : 4 times). Synopsys Design Compiler and Anam0.25 library is used for synthesis.

Table 1 Multiple specification Viterbi decoder Synthesis Result

	Multi Spec. Viterbi					Fixed Spec. Viterbi
	BMC	ACS	Systolic	Control	Total	
Area(gates)	89079	125381	145083	67	359610	311240
Timing (Critical path)	Timing Constraint : 20 ns Synthesis result : 19.80 ns					Timing Const. : 20ns Result : 19.80 ns

3.2 Simulation Results

Table 2 shows decoding performance of the multi spec. Viterbi and the fixed spec. viterbi. The simulation is executed using Matlab6.5 and Modelsim simulator. Target BER is 1.0×10^{-5} . Constraint length, soft decision bits, and decoding depth for the fixed specification Viterbi decoder are 7, 4, and 4, respectively. The simulation were performed on the 5×10^7 decoded bits.

In this simulation, the result BER is close to the target BER, which indicates that decoder works properly.

Table 2 Decoding performance and Specification

Eb/N0	Multi Spec. Viterbi		Fixed Spec. Viterbi
	Specification(Const. length , Depth)	Ave. BER	Ave. BER
1.3~1.7	(7,4) , (7,3)	9.6×10^{-6}	3.7×10^{-6}
1.4~2.2	(7,4) , (7,3) , (6,4) , (6,3)	9.7×10^{-6}	1.2×10^{-7}
1.6~2.7	(7,3) , (6,4) , (6,3) , (5,4) , (5,3) , (4,4) , (4,3)	1.0×10^{-5}	3.4×10^{-7}
1.6	(7,3)	7.2×10^{-6}	3.1×10^{-6}
1.3	(7,4)	9.2×10^{-6}	9.2×10^{-6}
1.1	(8,4)	1.0×10^{-5}	2.0×10^{-5}

4. Conclusion

In this paper, we propose an Viterbi decoder architecture with multiple specification. It can control the decoding parameters(constant length, decoding depth). This decoder provides 21 different specifications and can change its specification dynamically depending on the channel state. The proposed decoder is verified with simulation using matlab and modelsim simulator. The proposed Viterbi architecture has an area overhead of 16% more compare to traditional Viterbi decoder, but we can get stability of decoding performance by adjusting the specification.

Acknowledgement

This work was supported by grant No. RTI04-03-04 from the Regional Technology Innovation Program of the Ministry of Commerce, Industry and Energy(MOCIE) .

References

- [1] Savo Glisic, "Advanced Wireless Communications", John Wiley & Sons, Ltd., 2004.
- [2] Rahriema, M.; Antia, Y., Optimum soft decision decoding with channel state information in the presence of fading, Communications Magazine, IEEE, Vol. 35 pp.110-111 1997
- [3] F. Chan and D. Haccoun, "Adaptive Viterbi Decoding of Convolutional Codes over Memoryless Channels".IEEE Transactions on Communications, 45(11):1389-1400, Nov. 1997.
- [4] T. K. Truong et. al., "A VLSI Design for a Trace-Back Viterbi Decoder," IEEE. Trans. on Comm., vol. 40, pp.616-624, 1992.
- [5] Hanzo, L. and Liew, T. H., "Adaptive Coding and Transmission Paradigms for Wireless Channels", In Proceedings of 2nd IMA International Conference on Mathematics in Communications, pages pp.1-8, 2002
- [6] R. Henning and C. Chakrabarti " Low-power approach for decoding convolutional codes with Adaptive Viterbi Algorithm Approximations" Low Power Electronics and Design, 2002. ISLPED '02. Proceedings of the 2002 International Symposium on 2002 Page(s):68 – 71
- [7] Russel Tessier, Sriram Swaminathan, Ramaswamy Ramaswamy, Dennis Goeckel and Wayne Burleson, " A Reconfigurable, Power-Efficient Adaptive Viterbi Decoder" Very Large Scale Integration (VLSI) Systems, IEEE Transactions on Volume 13, Issue 4, April 2005 Page(s):484 - 488 2.