

A High Performance Flash ADC with Programmable Word-Length

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Abstract – Owing to its high complexity the hardware development of a flash ADC of larger word-length has always been a challenging issue. Being the fastest ADC available in practice, flash ADCs are the only solution for digitizing fast signals demanded by on-line real time digital processors. As computer designers have launched 64-bit machines into use, for real time processing applications they need word-length compatible flash ADCs. This paper reports the development of a programmable word-length flash ADC wherein the word-length in integer multiples of 8-bits is chosen by the user by opting a combination of 3-mini switches. The architecture for the large word-length flash ADC is built on a single 8-bit flash ADC producing progressively bit slice of 8-bits with the originating analog input and its subsequent residues. The progressive accumulation of bit slices contribute to the total word-length of the ADC. The conversion process terminates with those contribution of bit slices conceding word-length which meets the programmed ones. As the complexity of the proposed large word-length ADC is only slightly greater than that of 8-bit flash ADC and adaptable to the word-length of the system, it is promising to be useful for high speed real time digital processors.

Key words: flash ADC, programmable word-length, conversion time, circuit complexity, advanced architecture.

1. Introduction

Flash ADCs have proven to be the fastest ADCs available in practice. An inherent problem with the straight implemented flash ADC, however, is its circuit complexity. The circuit complexity gets doubled for every bit increase in the word length. Taking the complexity factor of 4-bit flash ADC as factor of one unit, the complexity encountered in 16-bit flash ADC would be 4K units and that of 32-bit flash ADC would be 256M units, the realization of which is far beyond the scope for implementation. In developing a high performance architecture for ADC, in the past, an architecture was reported for building high resolution ADC by using a low resolution flash ADC combined with another ADC of any type[1]. The speed of such devices would depend on the speed of the second ADC employed in this design as the first ADC being flash type it has only a little effect on the overall conversion time of the ADC. Based on this concept, with some changes in the circuits, a 16-bit ADC of one microsecond conversion time was developed and reported [2]. Although its complexity is much low compared to that of the flash ADC its speed is also lower compared to that of flash ADC. An improved architecture with built-in self-programming logic has been proposed[3] which has self-calibration features; but the resolution is only 10 bits. Another self calibrated ADC for improved speed has been reported [4] which again is meant for low-resolution converters. In showing up an improvement in the performance of the ADCs, fast compensating technique has been reported[5] which made the calibration process simplified. By and large, these improvements are concerning to the ADCs which are of low resolution types and not fast enough to accept large bandwidth signals such as video signals. In making attempts to reduce the complexity further, a high resolution flash ADC employing several low-resolution flash modules were reported[6,7]. The design was then improved by modifying the architecture and reported [8].

As modern computers are of 64-bit data word-length and they process information to produce high precision results. For processing real time signals of fast nature these computers need high resolution

flash ADC compatible to the word-length of the computer. Also in practice many digital machines processing fast real time signals may have lower word-lengths of data such as 8, 16 or 32 bits. Keeping in view of these system demands this paper reports a word-length programmable flash ADC which concedes the word-length for the ADC adjustable to any size demanded by the system. It is programmed by presetting a set of three mini switches before use. The architecture being efficient it results in a complexity much lower compared to that of conventional flash ADCs.

2. Advanced Architecture for Large Word-Length Flash ADC

By improving the architecture of the previous flash ADC [8] for reaching high resolution with reduced complexity, an efficient architecture is proposed now. In this architecture a large word length flash ADC (say 'n' bits) is built over a single flash ADC termed as stone ADC (say 'm' bits word length). Fig.1 shows its schematic where the m-b stone ADC is supported by 'p' numbers of latches to generate n-b word length. Incidentally the word length 'n' becomes the product of p and m.

$$n = p * m \tag{1}$$

There are p-1 number of m-b DACs and the same number of residue amplifiers in the structure. In front of ADC there is a p-ch analog MUX which takes any one of 'p' inputs to ADC as selected by the timing of p+1 phase clock generator. The gain of each residue amplifier is set as 2^m and remains constant. The ADC performs the conversion in 'p' phases generating each time a word slice of 'm' bits for the final digital word provided by the ADC. In the first phase of operation, it gets the most significant m-bit slice from the m-b stone ADC by taking the analog input v_i to it. In this phase the residue R_1 is generated by inverting v_i and feeding the analog equivalent of m-b data to the 1st residue amplifier. In the second phase of operation, the residue R_1 is fed to the stone ADC and the second m-b slice is obtained from it by producing the residue R_2 in a similar manner. This process continues and at the end, in the pth phase it concedes the least significant m-bit slice. Thus the word length of n-bits is successively realized with m-bit slice length in 'p' phases. While the first 'p' clocks arising from the clock generator are timing the respective phases in the ADC the last clock is used to denote the end of conversion.

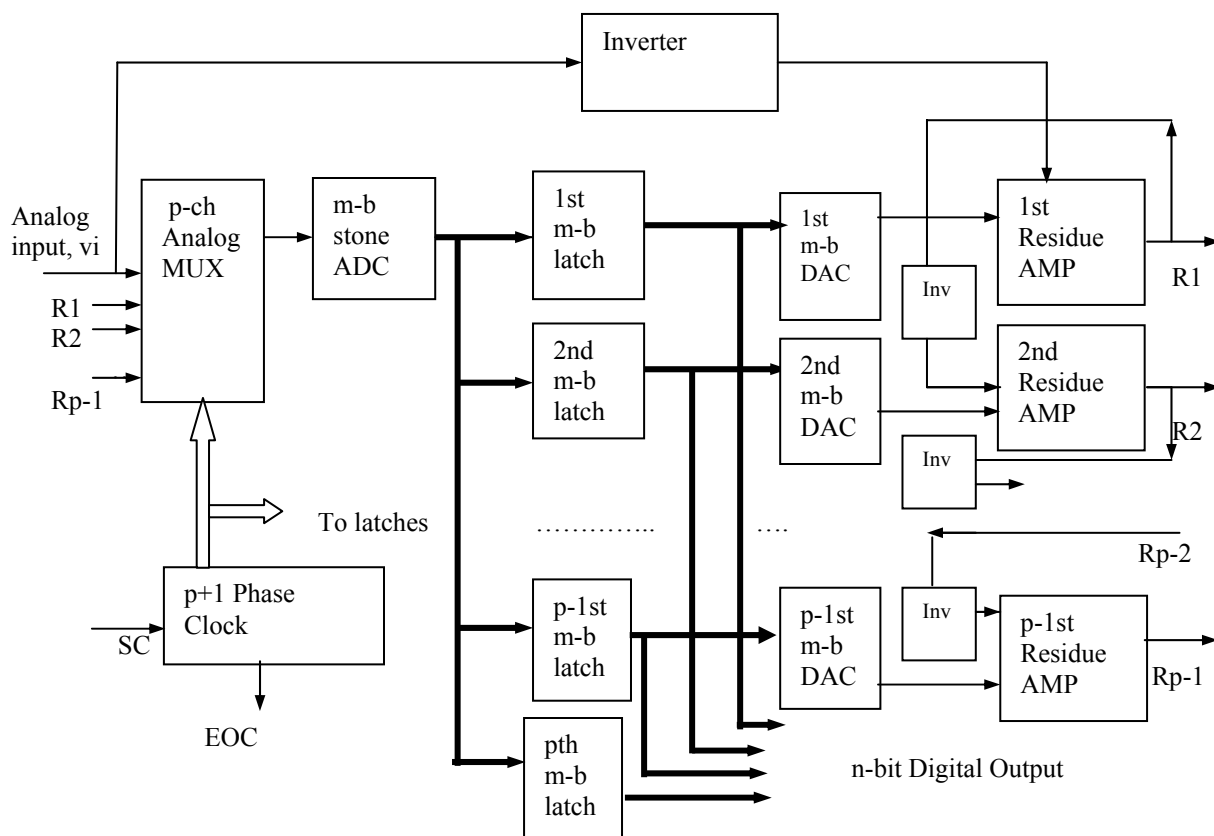


Fig.1 Advanced Architecture of large word-length ADC with accumulation of bit slices

3. Structure of Programmable Word-Length Flash ADC

In the proposed architecture of the flash ADC of conceding a maximum of 64 bits word-length we use one 8-b (m) flash ADC as the stone ADC, 8 (p) numbers of 8-b latches, 7 numbers of 8-b DACs and the same number of residue amplifiers as shown in Fig.2. For each residue amplifier, an 8-bit DAC provides one source and the other comes from the residue of the previous phase. For the residue amplifier 1, one input comes from the inverted version of v_i (the analog input) and the other input comes from the DAC output producing the analog equivalent of the most significant 8 bits. Therefore, the residue thus generated during the first phase is amplified by 256 (2^8) times and given as the analog input of the 8-b flash ADC for the second phase of operation. Likewise the residue generated in the second phase is also amplified by 256 times and given as the analog input for the third phase of conversion. This process continues until the eight phases are completed. A 9ϕ clock generator realized using cascaded mono-stable multi-vibrators is employed to produce the phasing signals.

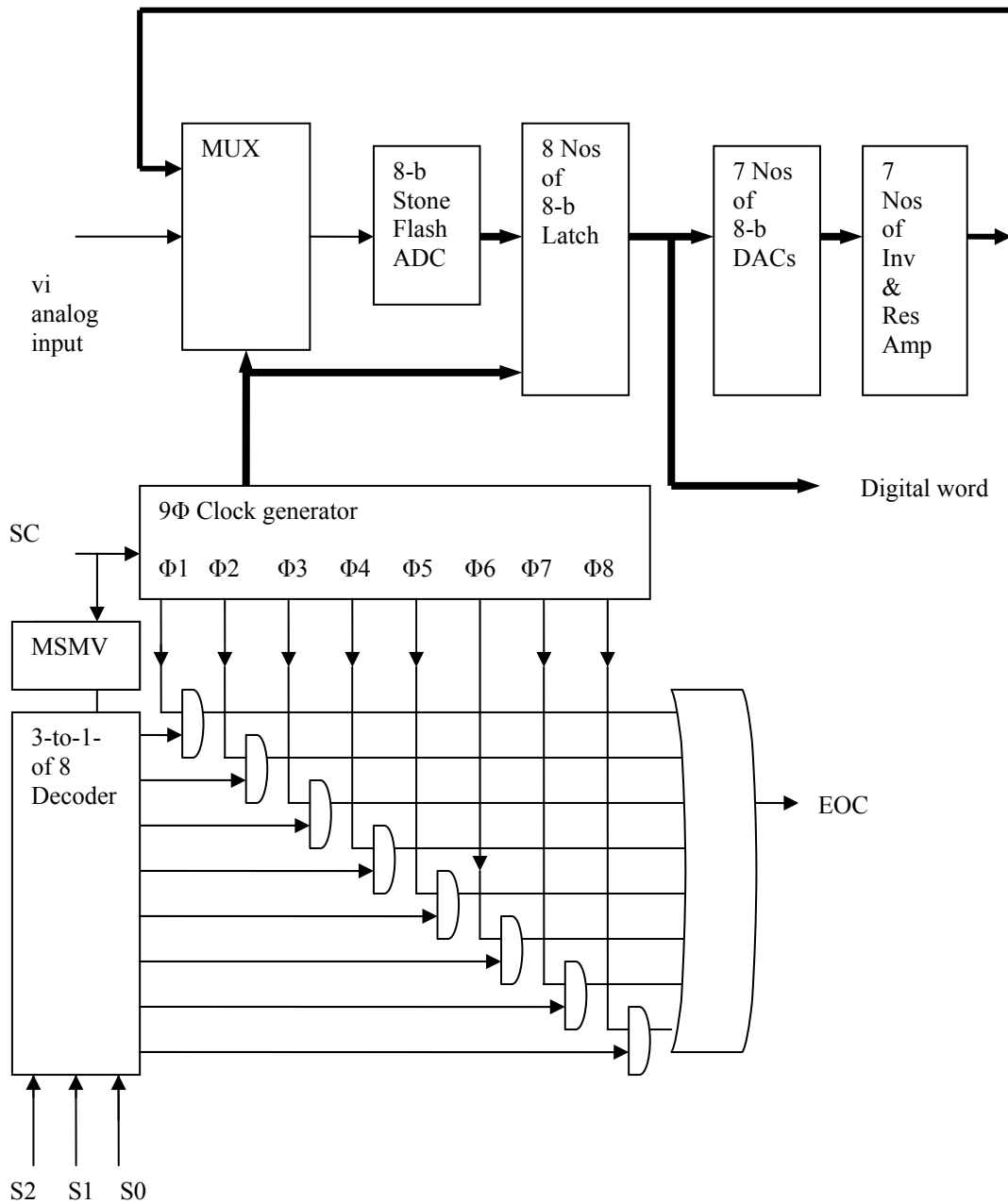


Fig.2. Structure of Programmable Word-length Flash ADC

The SC input triggers the phases to commence with 9Φ clock generator by entering into first phase of operation. The bit slice generation process from the 8-bit ADC commences by conceding the most significant 8 bits of the digital word of the ADC and progresses further. The conversion operation goes on until all eight phases are completed irrespective of the word-length programmed. However, the End of Conversion (EOC) signal is asserted after reaching the desired word-length. The next phasing clock arising after reaching the desired word-length is selected to be the EOC output for the ADC.

A set of three mini switches provide the word-length selection $S_2 S_1 S_0$ for the ADC. These 3-bits are decoded by 3-to-1-of-8 decoder as to select the phasing signal $\{\Phi_1 \Phi_2 \Phi_3 \Phi_4 \Phi_5 \Phi_6 \Phi_7 \Phi_8\}$ from the 9Φ clock generator as the EOC output. Obviously the external digital system uses the EOC to strobe the digital word to the system.

Having set the switches $S_2 S_1 S_0$ to be 011, as shown in Fig.2 the phasing signal Φ_4 would serve as the EOC signal of the ADC and its timing is indicated in Fig.3. The Monostable Multivibrator (MSMV) is triggered by the SC signal to produce a time slot T_c corresponding to 9 times of the clock period as to complete the worst case conversion and assert the EOC accordingly.

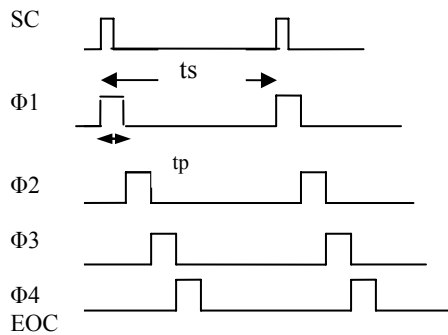


Fig.3. Timing diagram of the ADC for selection code 011
 t_s : sampling interval,
cycle time of ADC
 t_p : Phasing time

3.1. Residue Amplifier Structure

Fig.4 shows the structure of residue amplifiers used in the architecture. Only two stages are indicated in the figure. As seen in the figure, the output of the residue amplifier 1 is taken and given as one input of the residue amplifier 2 wherein another input for it comes from the DAC of the 2nd stage. The same configuration continues over all 8 stages. The gain of each residue amplifier being 256, the m^{th} residue amplifier amplifies the difference of $m-1^{\text{st}}$ residue output and the analog equivalent of the m^{th} digital bit slice by 256 times as to produce the residue of the m^{th} stage.

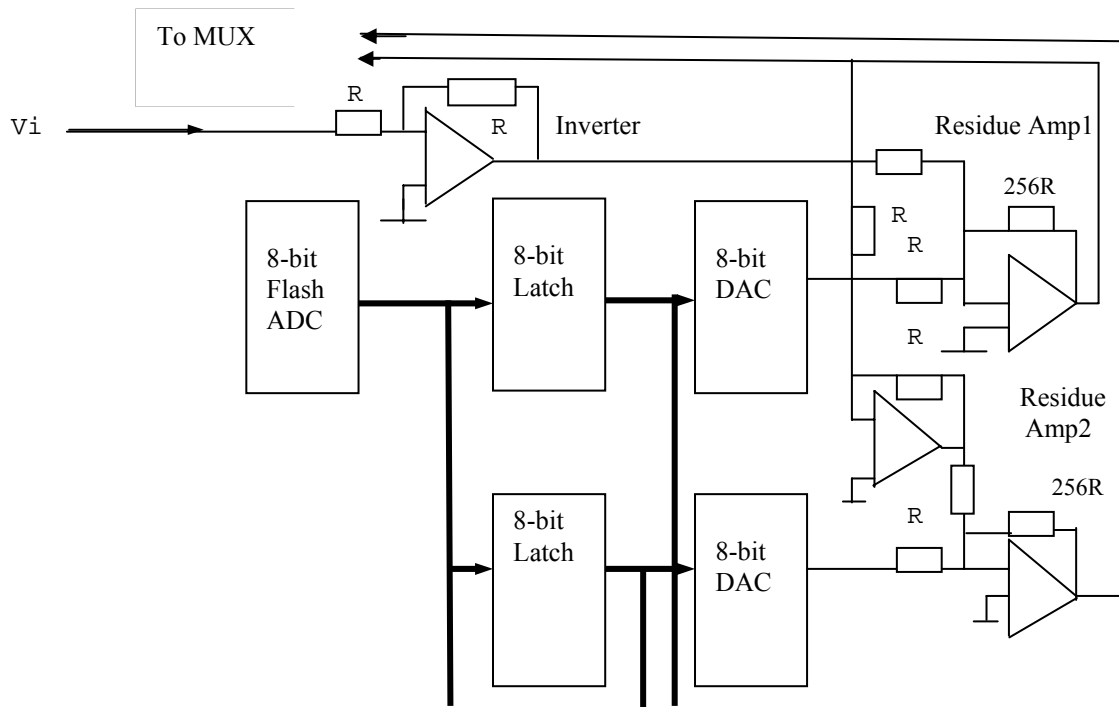


Fig.4. Structure of Residue Amplifiers

3.2 Conversion Time of 64-bit Flash ADC

In order to assess the performance of the ADC it is important to work out the conversion time of the 64-b flash ADC realized. The pulsing period 'tp' of the mono-stable multi-vibrators accounting for the period of each phase need be decided based on the total delay contributed by various circuits in the structure. The pulsing period tp is given by

$$t_p = t_m + t_c + t_l + t_{dac} + t_r \quad (2)$$

where 'tm' is the delay caused by the analog multiplexer, 'tc' the conversion time of the 8-bit flash ADC, 'tl' the latching delay, 'tdac' the delay caused by the settling time of the DAC and 'tr' the delay due to the settling time of the residue amplifier.

These delay periods in the circuits depend on the technology employed in fabricating the devices. With the recent growth in technology these delays can be as low as few nanoseconds[9-11] shown in table 1. The time needed for each phase 'tp' turns out to be 10ns to allow all delay times encountered in the phase and the total conversion of the ADC including the period of the EOC becomes 80ns. The conversion time of the ADC depends on the word-length programmed for the ADC.

$$T_c = n_p * t_p \quad (3)$$

Where 'np' is number of phases involved in reaching the desired word-length.

For continuous sampling of the signal such as in digitizer, next sample has to be made after the conversion time Tc. This causes the maximum sampling frequency to be that of 1/ Tc. Fig.5 shows the relationship between the programmed word-length of the ADC and the maximum sampling frequency possible.

Table 1. Typical delay times of recent devices

Parameter	Delay time (ns)
tm	2
tc	3
tl	1
tdac	2
tr	2

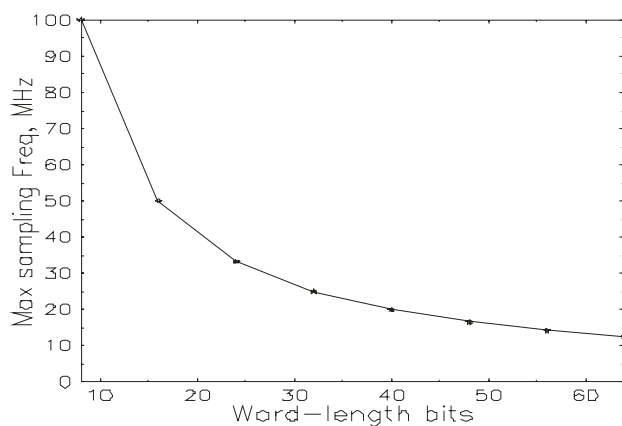


Fig.5. Relationship between Sampling Frequency and Word-Length

4. Conclusion

A novel architecture is reported for building high resolution flash ADC using just one low resolution flash ADC. Increase in word size of the proposed flash ADC results in only a little increase in the complexity trading off with conversion time to a little extent only. The high resolution ADC of the maximum word length of 64-bits realized has proved to show less complexity and moderate high speed compared to the previous designs. The word-length is programmable to the needs of any processor in use. The complexity of the 64-b ADC is only slightly greater than that of the 8-b flash ADC resulting in a slight increase in conversion time which is affordable to most high frequency signals. As the propagation delay resulted in 8-b flash ADC is considerably low due recent growth in technology, the total conversion time of the 64-b ADC is just 80ns only. It is to be noted that when the word-length is relatively lower it concedes relatively increased sampling frequency due to the relatively reduced conversion time. This therefore satisfies the requirements of modern digital computers to get the fast analog signals digitized to the word-length compatible to the word-size of the processor and makes itself adapted to any digital processor irrespective of its data word-length.

Acknowledgement

The author acknowledges with thanks all necessary support extended by the Department of Computer Engineering for carrying out this project. He also thanks the Faculty of Architecture and Engineering and the Rector of European University of Lefke for providing the funding support for the development of some parts of the project.

References

- [1]. K.Balasubramanian, "Improving the resolution of selected ADCs", IEEE Trans on Consum Electron, Vol 37, No 1, pp 81-85, 1991.
- [2]. K.Balasubramanian and H.Camur, "1 μ s, 16-bit analogue-to-digital converter", Electronics World, Vol 105, No 1755, pp 242, 1999.
- [3]. Giovanni Bucci, Marco Faccio and Carmine Landi, "Advanced ADC architecture with built-in self programming logic", Proceedings of the 1999 IEEE Instrumentation and Measurement Technology Conference, Venice, Italy, pp 1299-1304, 1999.
- [4]. Andrea Boni and Andrea Pierazzi, "Self calibrating input interface for high speed low power differential ADCs", Proceedings of the 1999 IEEE Instrumentation and Measurement Technology Conference, Venice, Italy, pp 1290-94, 1999.
- [5]. G.M.Kelso, D.M.Hummels, and F.H.Irons, "Fast compensation of Analog to Digital Converters", Proceedings of the 1999 IEEE Instrumentation and Measurement Technology Conference, Venice, Italy, pp 1295-1298, 1999
- [6]. K.Balasubramanian, "High resolution A-to-D using low resolution converters", Electronics World, pp 1052, 1991.
- [7]. K.Balasubramanian, "A flash ADC with reduced complexity", IEEE Trans. on Ind. Electron, Vol 42, No 1, pp 106-108, 1995.
- [8]. K.Balasubramanian, "On the design and development of flash ADCs", Journal of AMSE-Modelling Measurement and Control, A-series, France, 2003, Vol 76, No. 5, pp 31-43.
- [9]. Analog Devices Corporation's Data Acquisition Catalogue, MA, USA, 1988.
- [10]. Texas Instruments Semiconductor Master Selection Guide, Bedford, UK, 1986.
- [11]. National Semiconductor's Semiconductor Master Selection Guide, Santa Clara, CA, USA, 1988.